



Nanoelectronics on Si

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近年奈米科技之發展

- 縮小尺度至100 nm以內的科技：
Top-down之奈米結構的雕刻細化
莫爾定律(Moore's law—每1.5年縮小30%尺寸)
- 操控原子（分子）的科技：Bottom-up 之
奈米體系的成長組裝
費曼的主張—從底部作起，下面還有無限寬廣的空間



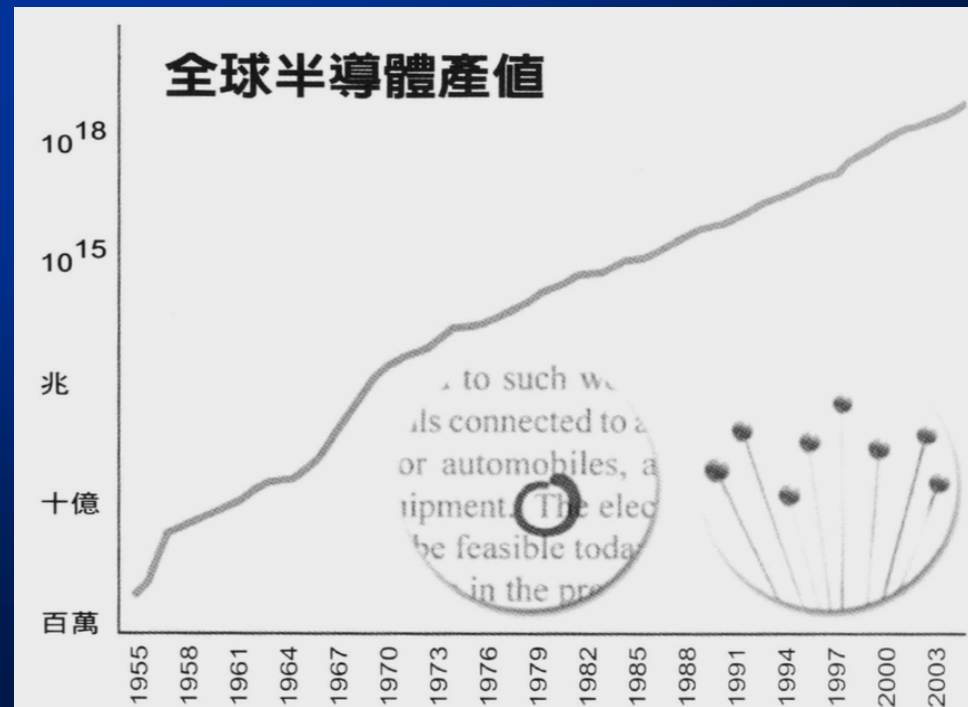
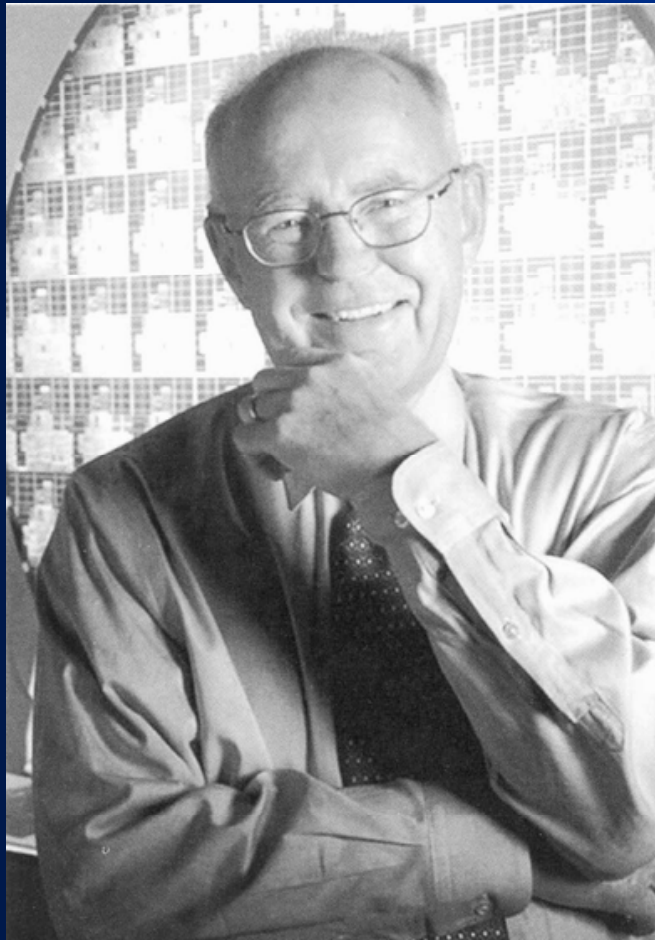
近來大力推動奈米科技的背景

來自微電子學可能遭遇瓶頸的考慮

Moore's Law：摩爾定律

A 30% decrease in the size of
printed dimensions every 1.5 years.

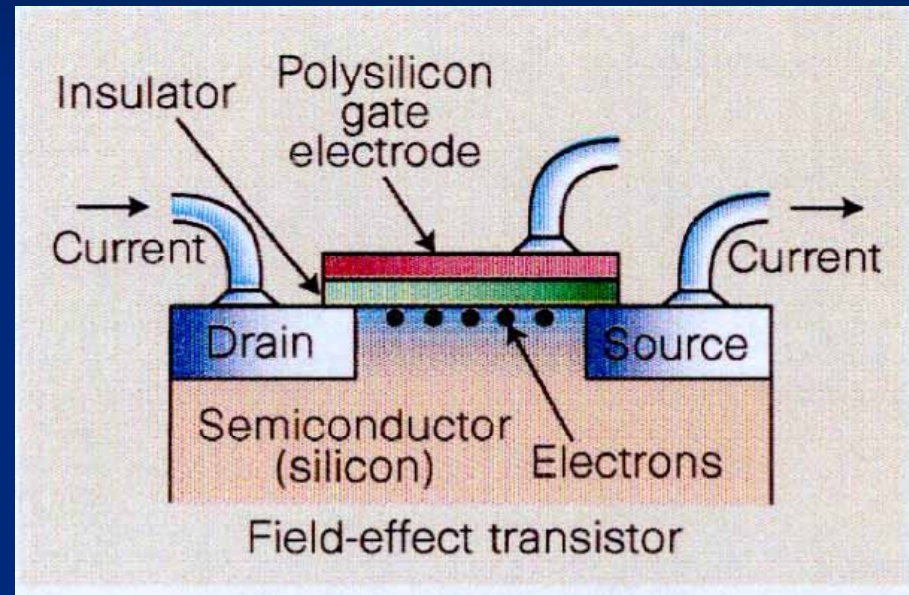
矽晶上電子原件數每1年半會增加一倍





Device Scaling, Moore's Law

1960 Kahng and Atalla, First MOSFET



Moore's Law:

The number of transistors per square inch doubles every 18 months

Shorter gate length L

Thinner gate dielectrics t_{ox}

Driving force :

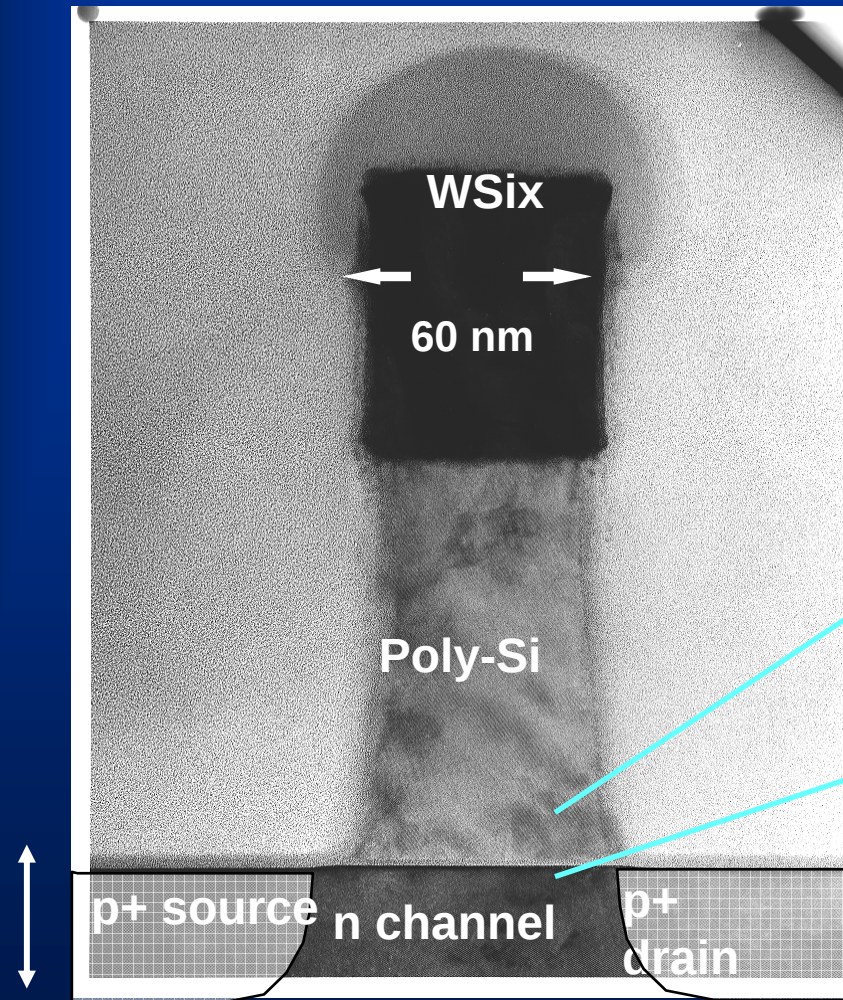
High speed

Lower power consumption

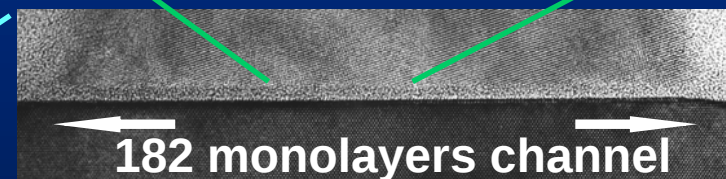
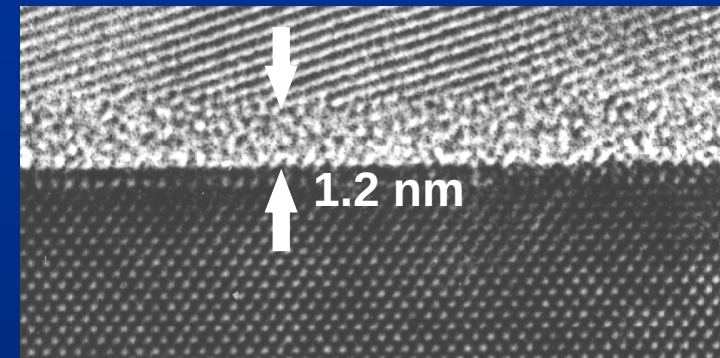
High package density



Scaling Limits to CMOS Technology



Gate Oxide ~ 5 Si Atoms thick !



Shrinking the junction depth → increasing the carrier concentration



Intel Transistor Scaling and Research Roadmap

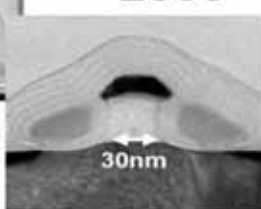
Transistor Scaling and Research Roadmap

90nm Node
2003



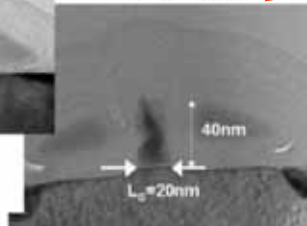
50nm Length
(Production)

65nm Node
2005



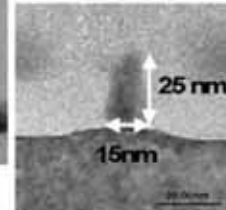
30nm Length
(Development)

45nm Node
2007



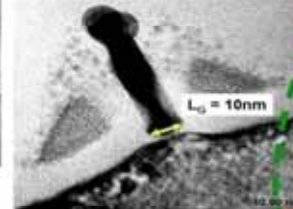
20nm Length
(Development)

32nm Node
2009



15nm Length
(Research)

22nm Node
2011

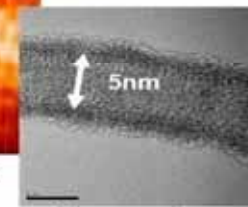


10nm Length
(Research)

2015-2019
Research



III-V Device
Prototype
(Research)



C-nanotube
Prototype
(Research)

Nanowire
Prototype
(Research)

Uniaxial
Strain

SiGe S/D PMOS

1.2nm Ultra-thin SiO₂

High-K &
Metal-Gate
Options

Non-planar Tri-Gate
Architecture Option

Robert Chau, Intel, ICSICT 2004

More non-silicon elements introduced

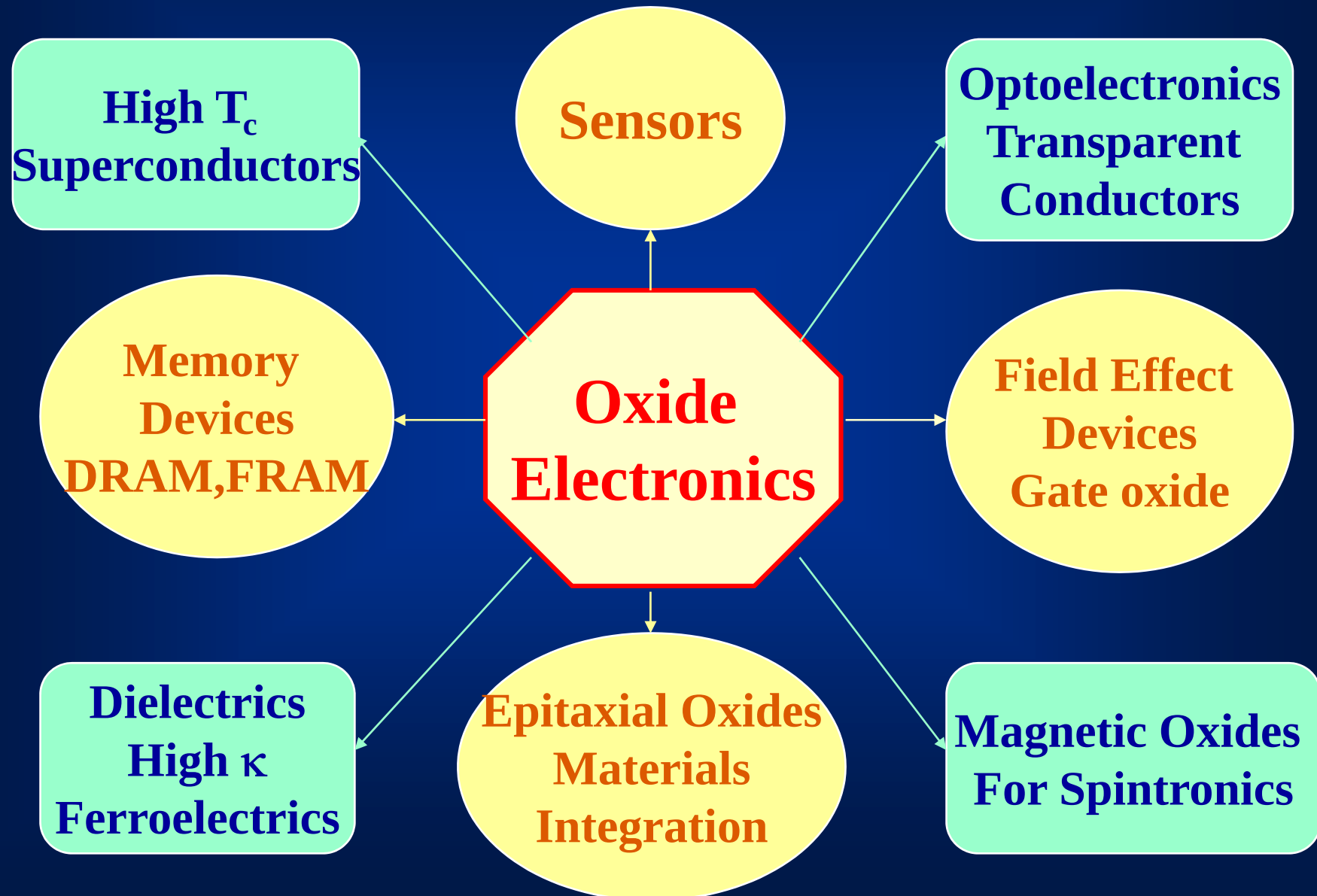


OUTLINES

- ❖ The alternative high κ gate dielectrics replacing SiO_2 for 33 nm Si CMOS by year 2009
 - Materials requirements
 - Processing integration issues
- ❖ MBE grown HfO_2 high κ gate dielectrics
 - thermal stability studies by MEIS and TEM
 - electrical performance
- ❖ Integration of ALD + MBE template approach



The Development of Oxide Electronics in Two Decades





CMOS scaling, When do we stop ?

Reliability: 25 ~~22~~ ~~18~~ ~~16~~ Å

processing and yield issue

Tunneling : 15 Å

Design Issue: chosen for 1 A/cm² leakage

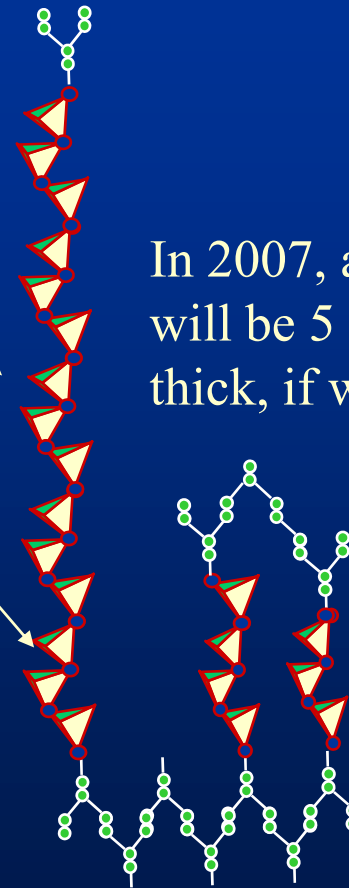
$I_{\text{on}}/I_{\text{off}} \gg 1$ at 12 Å

Bonding:

Fundamental Issues---

- how many atoms do we need to get bulk-like properties?
EELS -- Minimal 4 atomic layers !!
- Is the interface electronically abrupt?
- Can we control roughness?

In 1997, a gate oxide was 25 silicon atoms thick.

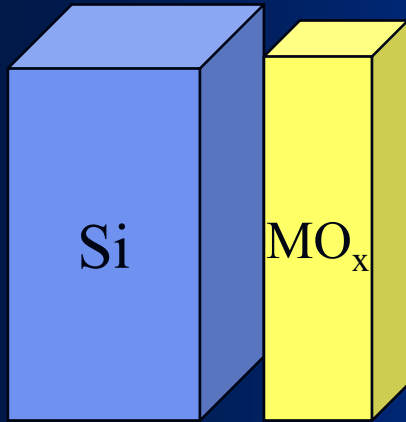


In 2007, a gate oxide will be 5 silicon atoms thick, if we still use SiO₂

and at least 2 of those 5 atoms will be at the interfaces.



Fundamental Materials Selection Guidelines



- Thermodynamic stability in contact with Si to 750°C and higher. **(Hubbard and Schlom)**
Alkaline earth oxide, IIIB, IVB oxide and rare earth oxide
- Dielectric constant, band gap, and conduction band offset
- Defect related leakage,
substantially less than SiO_2 at $t_{\text{eq}} < 1.5 \text{ nm}$
- Low interfacial state density $D_{\text{it}} < 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$
- Low oxygen diffusivity
- Crystallization temperature $> 1000^\circ\text{C}$

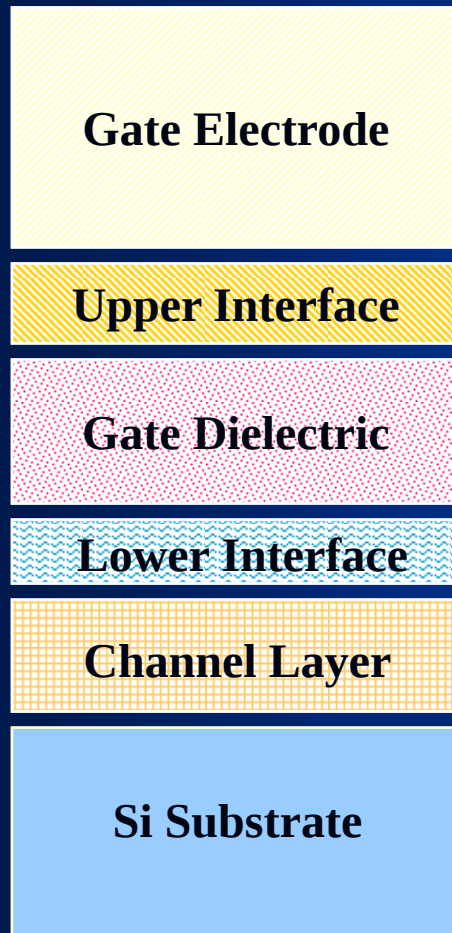
t_{eq} : **equivalent oxide thickness (EOT) to be under 1.0 nm**

$$t_{\text{eq}} = t_{\text{ox}} \kappa_{\text{SiO}_2} / \kappa_{\text{ox}}$$



Integration Issues for High κ Gate Stack

FET Gate Stack



Critical Integration Issues

- Morphology dependence of leakage
Amorphous vs crystalline films?
- Interfacial structures
- Thermal stability
- Gate electrode compatibility
- Reliability

Fundamental Limitations

- Fixed charge
- Dopant depletion in poly-Si gate
- Dopant diffusion
- Increasing field in the channel region



Basic Characteristics of Binary Oxide Dielectrics

Dielectrics	SiO ₂	Al ₂ O ₃	Y ₂ O ₃	HfO ₂	Ta ₂ O ₅	ZrO ₂	La ₂ O ₃	TiO ₂
Dielectric constant	3.9	9.0	18	20	25	27	30	80
Band gap (eV)	9.0	8.8	5.5	5.7	4.5	7.8	4.3	3.0
Band offset (eV)	3.2	2.5	2.3	1.5	1.0	1.4	2.3	1.2
Free energy of formation MO _x +Si ₂ → M+ SiO ₂ @727C, Kcal/mole of MO _x	-	63.4	116.8	47.6	-52.5	42.3	98.5	7.5
Stability of amorphous phase	High	High	High	Low	Low	Low	High	High
Silicide formation ?	-	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Hydroxide formation ?	-	Some	Yes	Some	Some	Some	Yes	Some
Oxygen diffusivity @950C (cm ² /sec)	2x 10 ⁻¹⁴	5x 10 ⁻²⁵	?	?	?	10 ⁻¹²	?	10 ⁻¹³

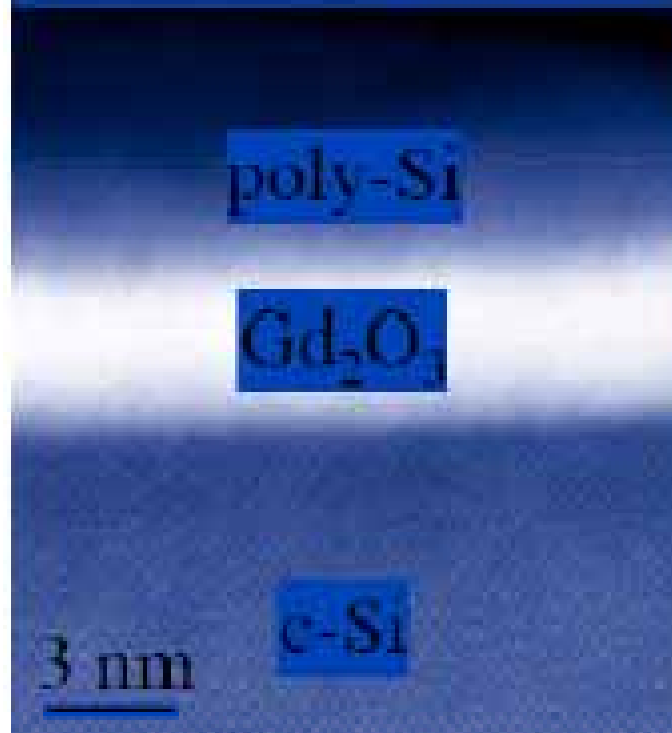
Assessing Thermodynamic Stability

Gate Dielectric
Material

Silicon

Ideal
“Gedanken”
Interface

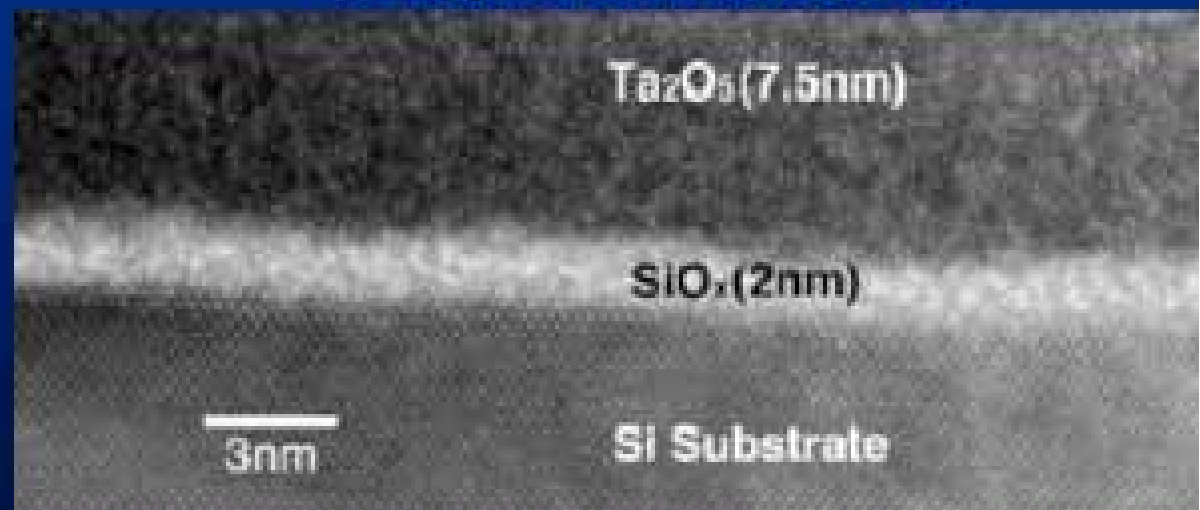
Stable Interface



TEM by David A. Muller

J. Kwo *et al.*, J. Appl. Phys. 89 (2001) 3920.

Unstable Interface



TEM by Don J. Werder

G.B. Alers *et al.*, Appl. Phys. Lett. 73 (1998) 1517.



Band Offset of High κ Dielectrics

Band Offsets of Dielectrics with Si



J. Roberson, JVST 18, 1785, (2000)



A Topic Well Worth Doing Research On !!!

World production in year 2003: 1×10^{19} transistors

World population: 6.4×10^9 people

So, the world produces:

$\sim 1.5 \times 10^9$ transistors/person each year

$\sim 1.2 \times 10^8$ transistors/person each month

$\sim 4\text{M}$ transistors/person each day

$\sim 3\text{K}$ transistors/person each minute

~ 50 transistors/person per second

And Taiwan produces ~ 5000 transistors/person/per second



MBE Integrated Multi-chamber System For Nano Electronics

Si gate oxide growth



Now located in the Nano
Technology Center, ITRI,
Hsin Chu, Taiwan since
7/2003.

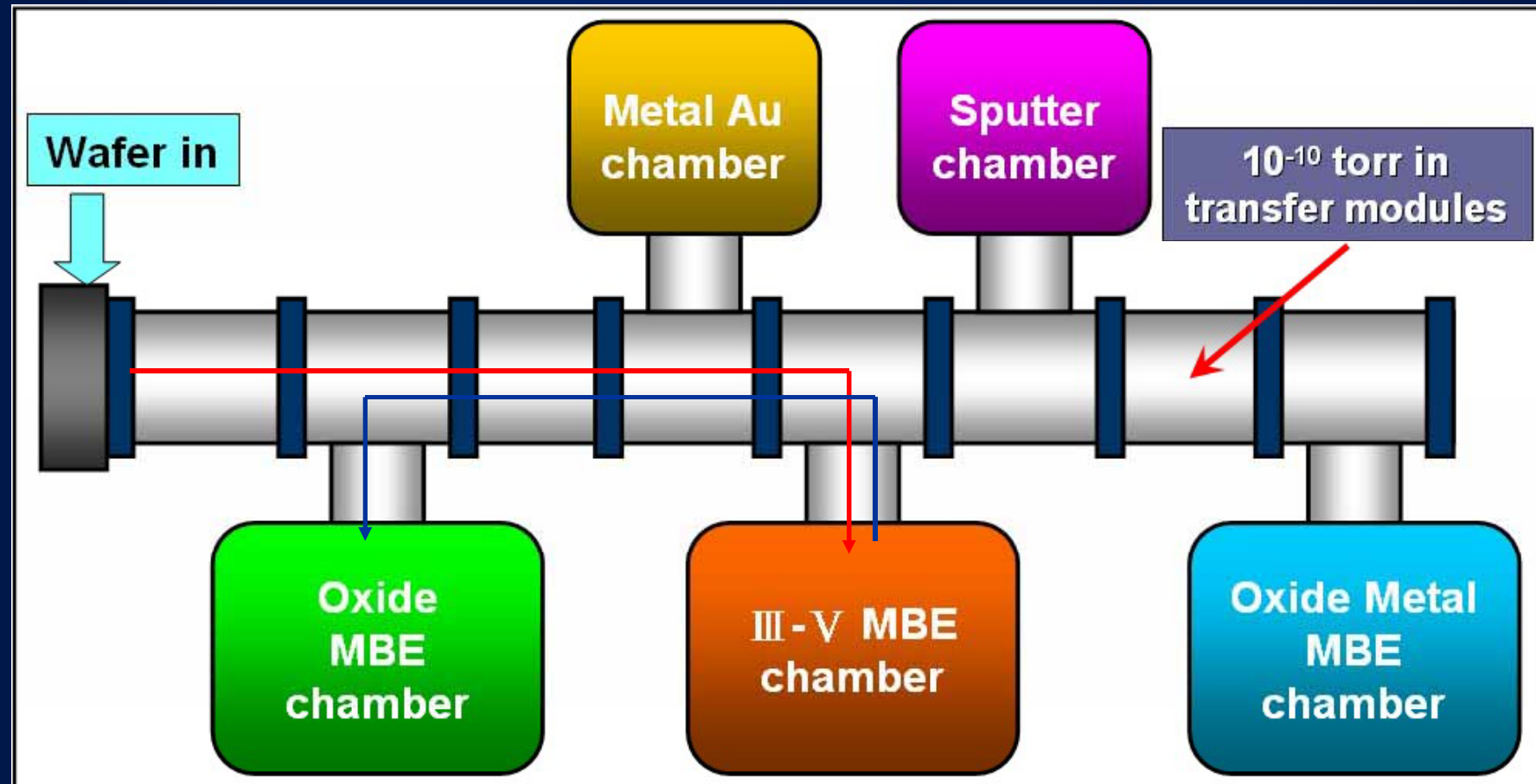
III-V gate oxide growth





In-situ Fabrication

UHV integrated processing system

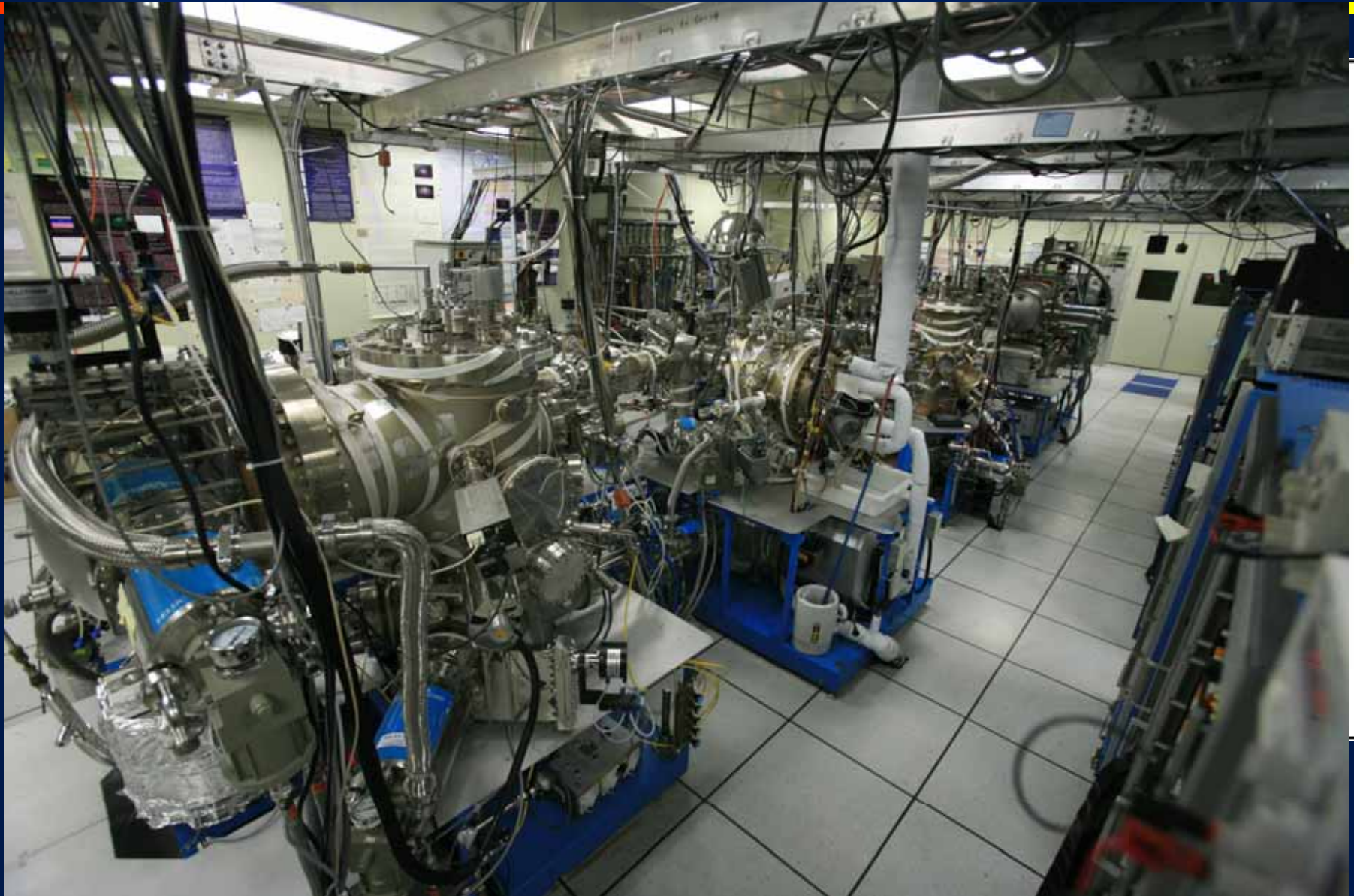


Multichamber Ultrahigh Vacuum System

1. A solid source GaAs-based MBE chamber
2. Oxide deposition chamber (As-free)
3. UHV transfer modules



In-situ Fabrication



3. OTV transfer modules



High κ Dielectrics for Si

■ Epitaxial crystalline films on Si

(A) Cubic CaF_2 structure:

(111) orientation is more common than (100)

e.g. CaF_2 (111), CeO_2 (111) on Si(111) with $\epsilon \sim 26$

YSZ (100) on Si(100) with $\epsilon \sim 25-30$

(B) Cubic Mn_2O_3 structure

~ 8 unit cells of incomplete fluorite structure

e.g. Y_2O_3 (110) on Si(100) with $\epsilon \sim 16-18$

Gd_2O_3 (110) on Si(100) with $\epsilon \sim 12-14$

(C) Ternary perovskite structure

e.g. SrTiO_3 (100) on Si(100) with $\epsilon \sim 70-80$ (Oakridge, Motorola)

using a Sr silicide $\frac{1}{4}$ monolayer for epi-growth

■ Amorphous oxide films on Si

e.g. Si_3N_4 , Al_2O_3 , Ta_2O_5 , ZrTiSnO_x , TiO_2 Interfacial layer present

- Amorphous Gd_2O_3 and Y_2O_3 films

- Amorphous SiO_2 added with Hf or Zr. (G. Wilks et al)



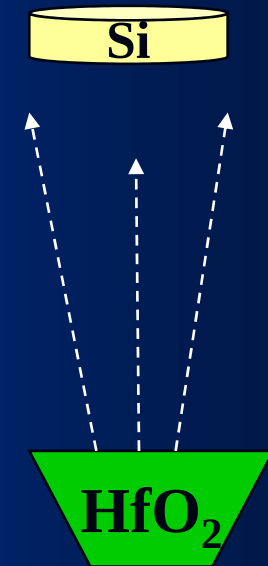
Research Programs

- Low defect high κ ultrathin films
 - Interface engineering
 - Electrical characterization and optimization
- Identify new material candidates for metal gate
 - Metal gate/high κ integration
- Integration of high κ , and metal gate with Si- Ge strained layer
Integration of high κ , and metal gate with strained Si
- High k dielectrics for high mobility III-V semiconductors



MBE Growth of High κ Oxides

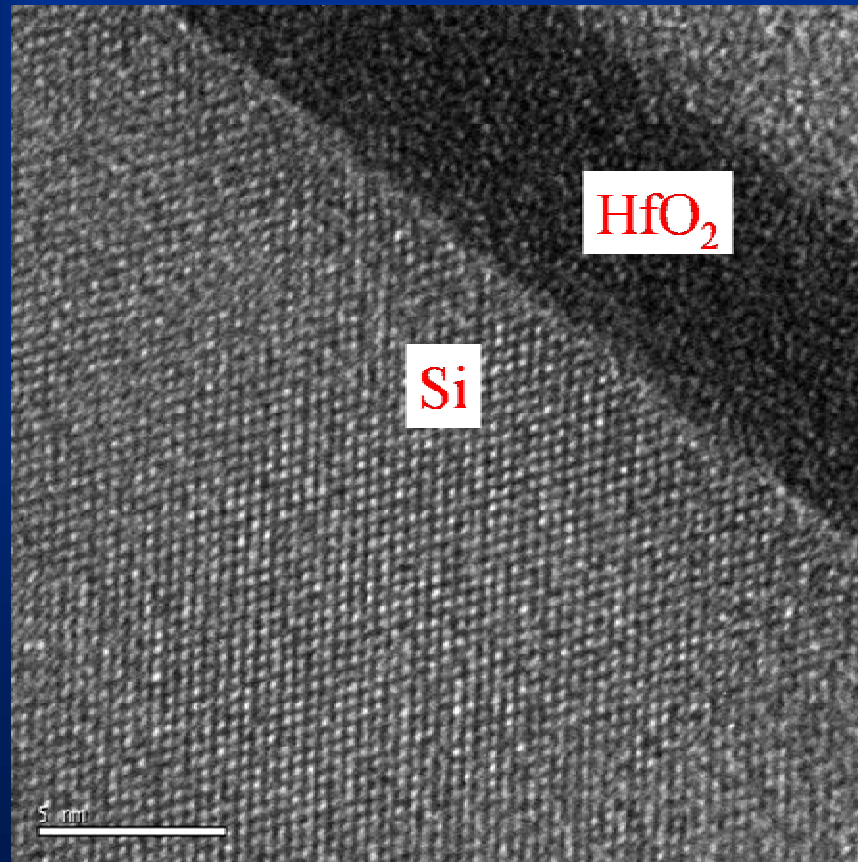
- Ultrahigh vacuum, multi-chamber MBE system.
- Electron-beam evaporation of oxide sources from pressed ceramic pellets.
- 2 inch RCA-cleaned Si wafers, hydrogen passivated, followed by prompt insertion into UHV.
- In-situ heating to 400-500C to attain a (2 x 1) reconstructed Si surface.
- Substrate temperature of 550C for **epitaxial** films.
- Room temperature deposition for **amorphous** films.
- Maintain **low pressure** during growth $< 1.0 \times 10^{-9}$ torr.





High Resolution Cross Sectional TEM and RHEED Images of HfO_2 on Si (100)

From AFM: RMS Roughness: 0.072nm



Amorphous HfO_2 film 6.0 nm
 SiO_2 and Hf silica is nearly absent !

RHEED



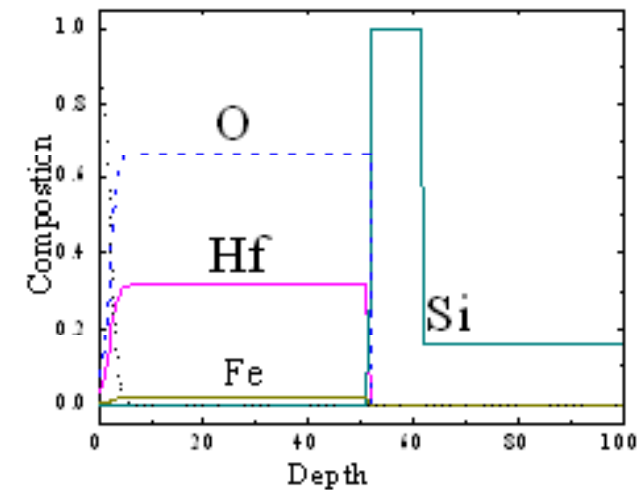
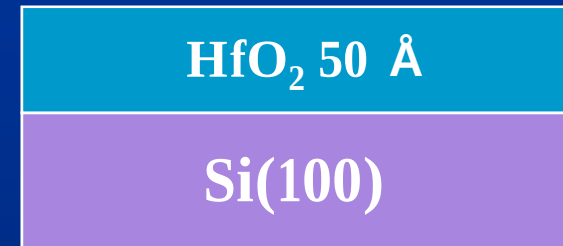
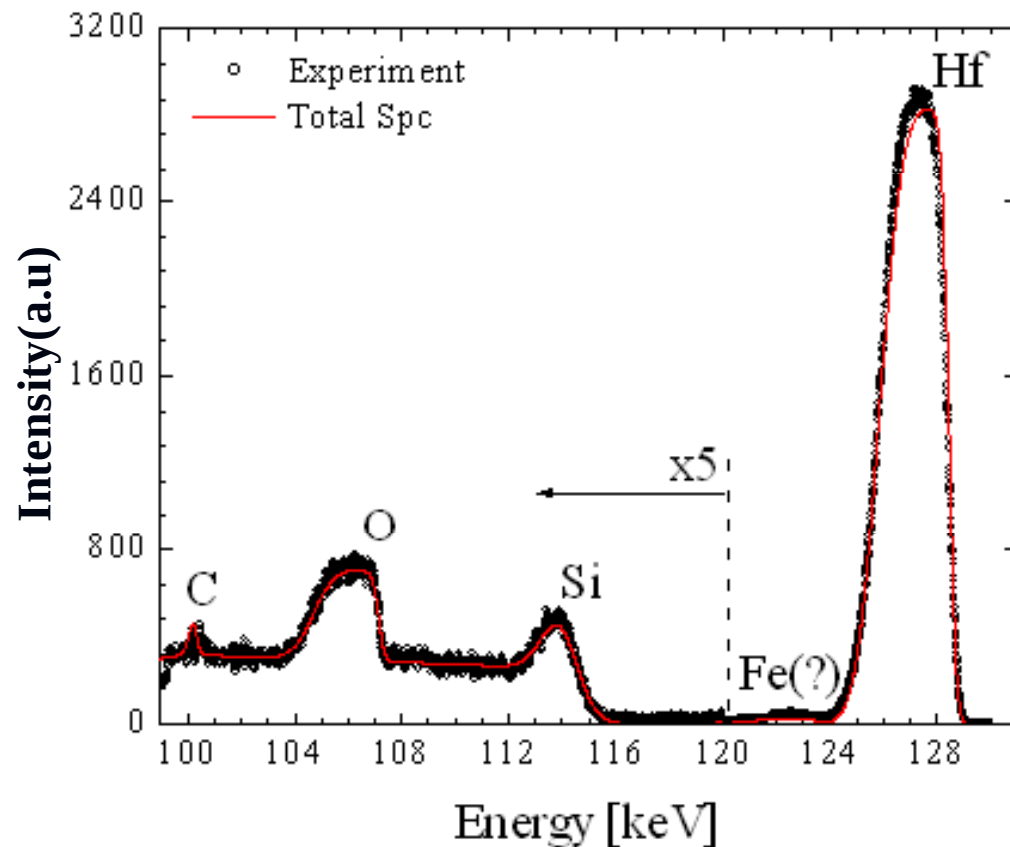
amorphous HfO_2 surface



atomically order Si(100) surface



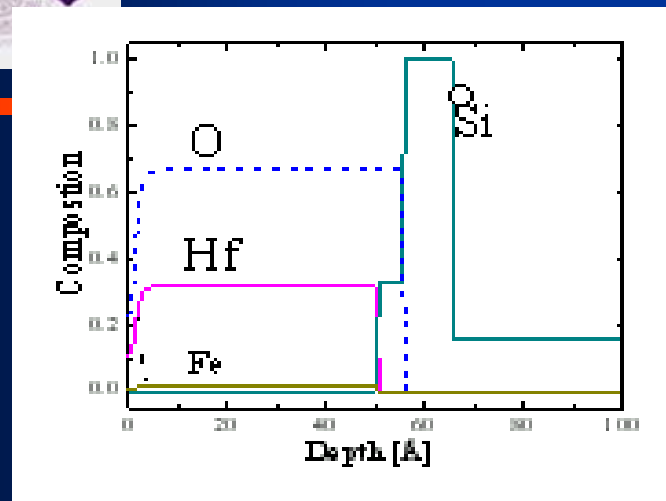
Medium Energy Ion Scattering (MEIS) Study of the High κ Dielectric / Si Interface and Stability



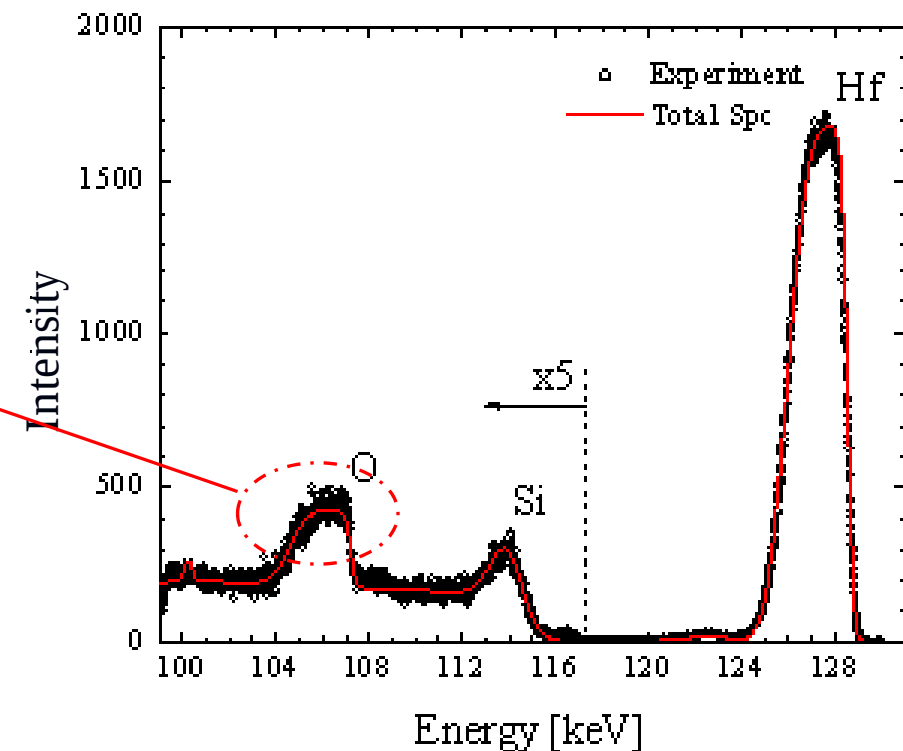
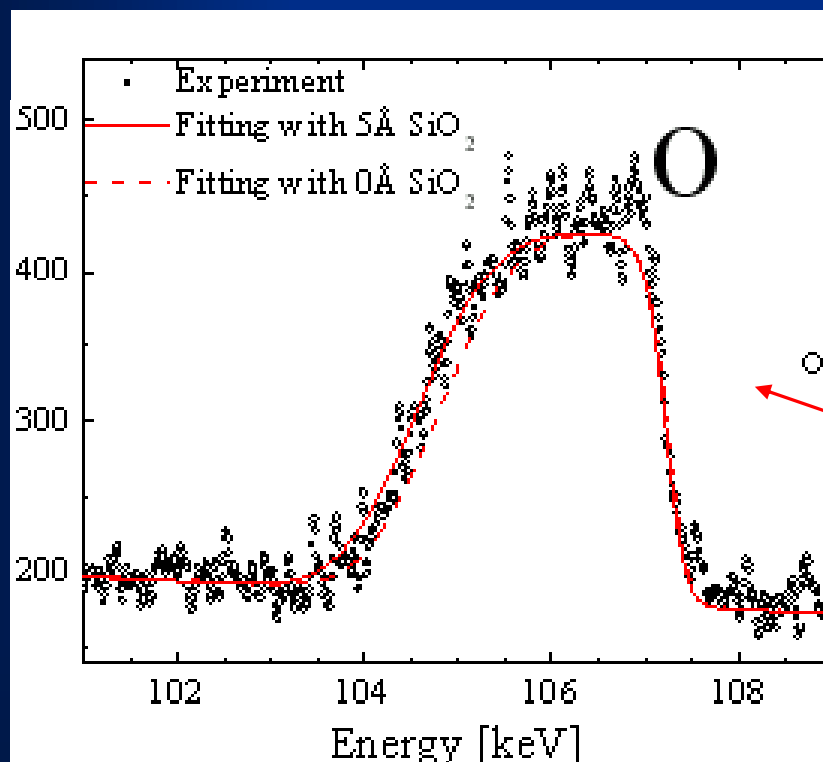
With Rutgers University using 130 keV proton beam
It shows the absence of silica near the interface.



Vacuum annealing at 630°C

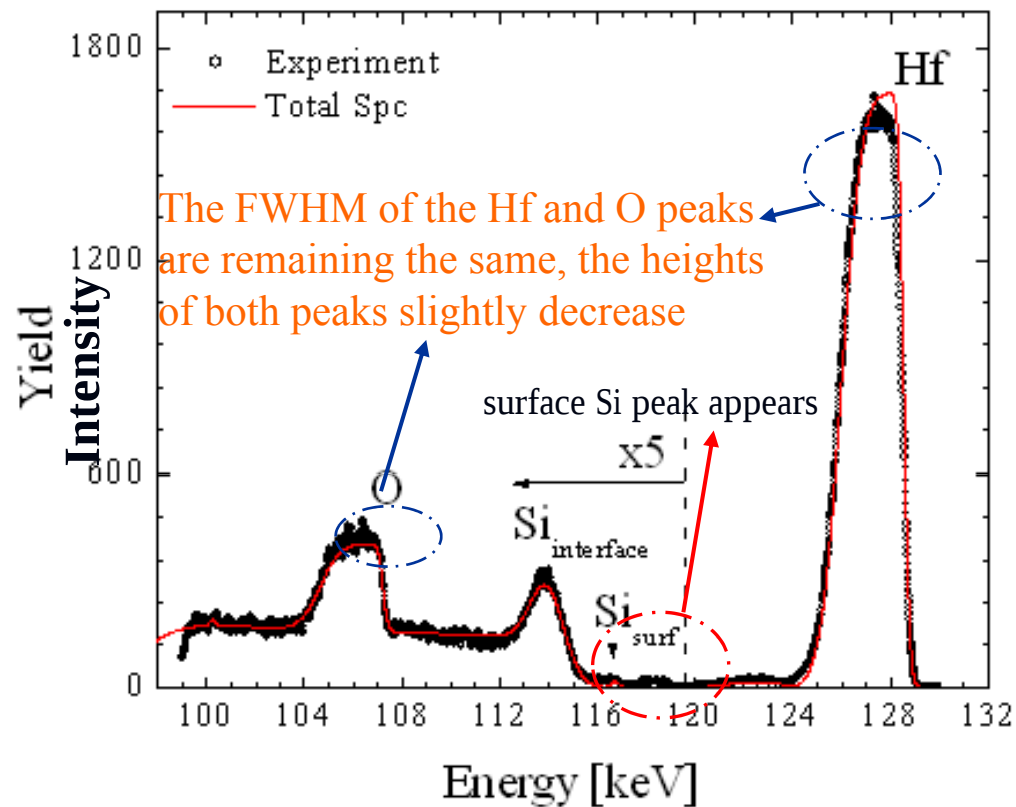


Broadening of the O peak and small increase in the Si peak indicate some interfacial SiO_2 formation about 0.4 nm.





Annealing from 630°C to 950°C



A possible structure after high temperature anneal

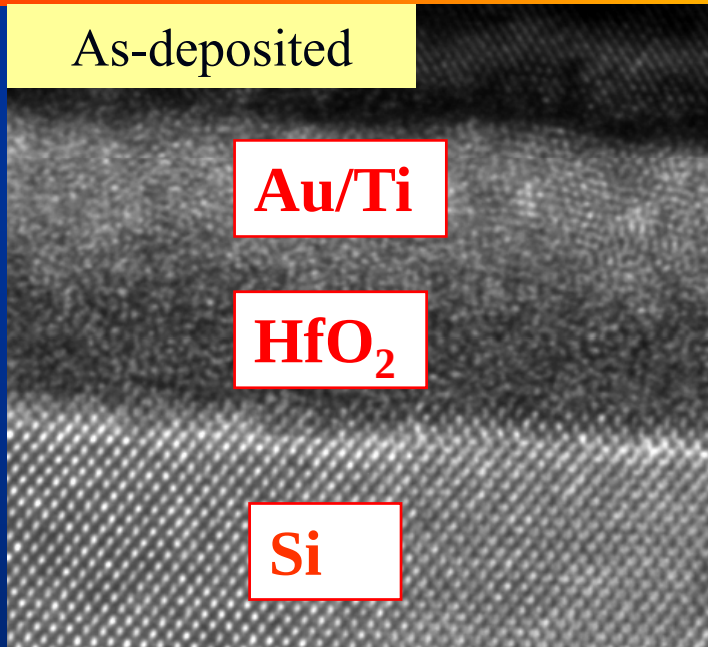


Discontinuities and islands were formed in HfO₂.



HRTEM Study of Thermal Stability of High κ HfO₂ Gate Stacks

As-deposited

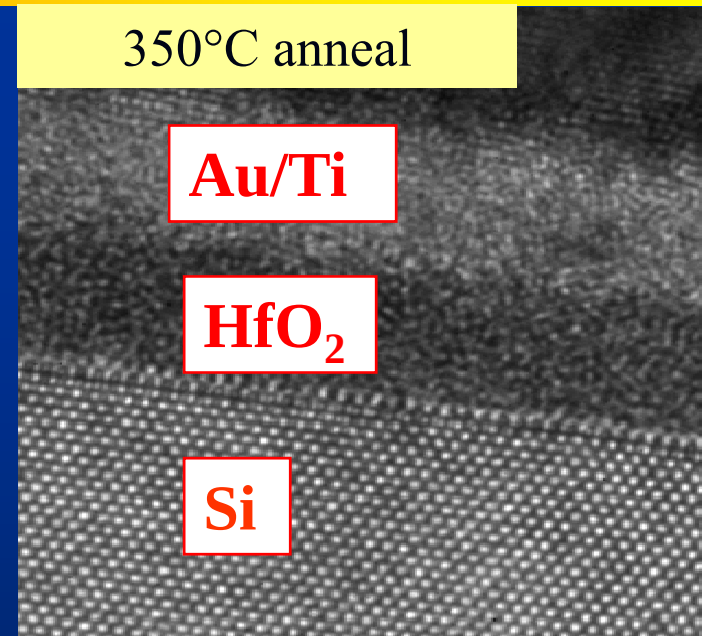


Au/Ti

HfO₂

Si

350°C anneal

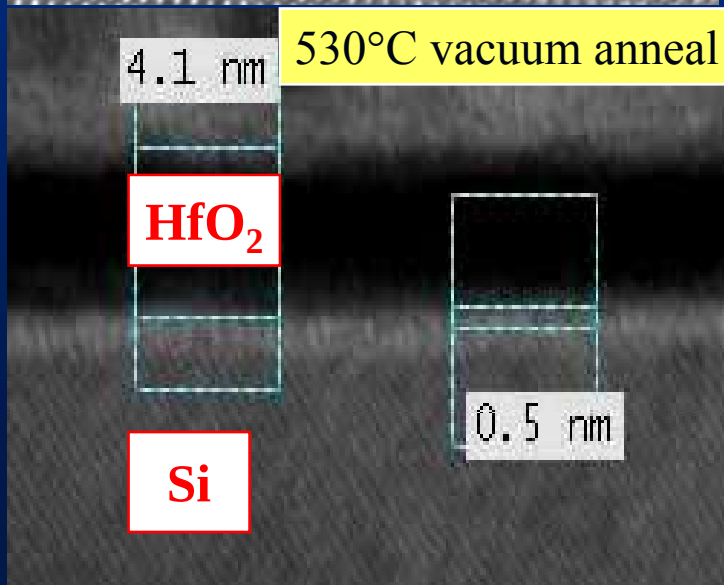


Au/Ti

HfO₂

Si

530°C vacuum anneal



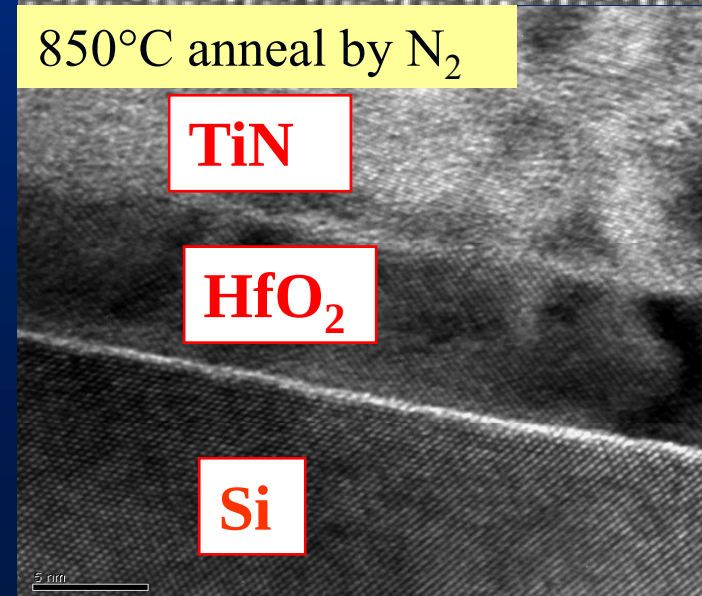
4.1 nm

HfO₂

Si

0.5 nm

850°C anneal by N₂



TiN

HfO₂

Si

5 nm



Difficulties of High κ MOSFET Fabrications

- Thermal stability of thin films
 - HfO_2 → Lowering the dopant activation temperature to 700°C
 - TiN → Using Ti/TiN bilayer structure
- Process integration
 - 4 inch Si (LOCOS) → 2 inch Si (MBE)
 - Successful integration

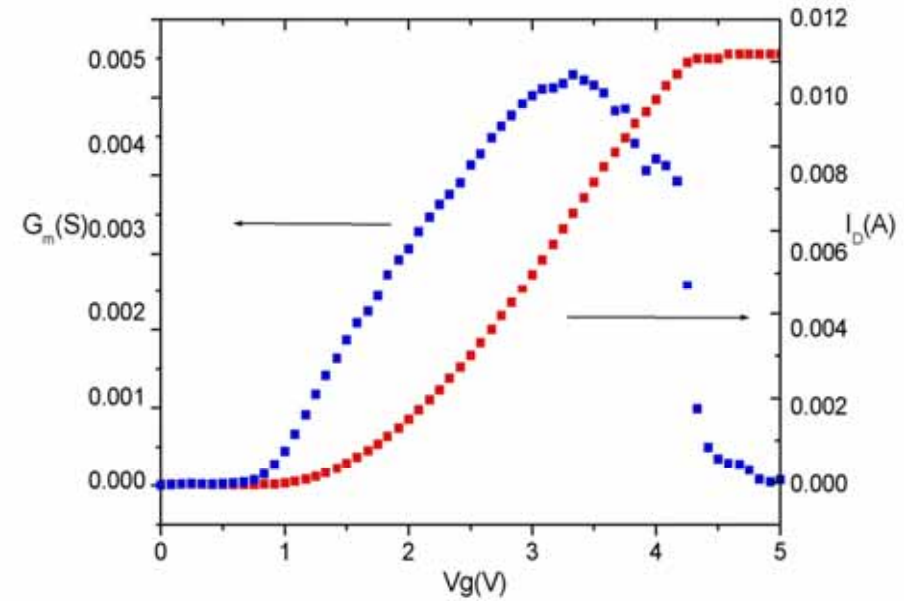
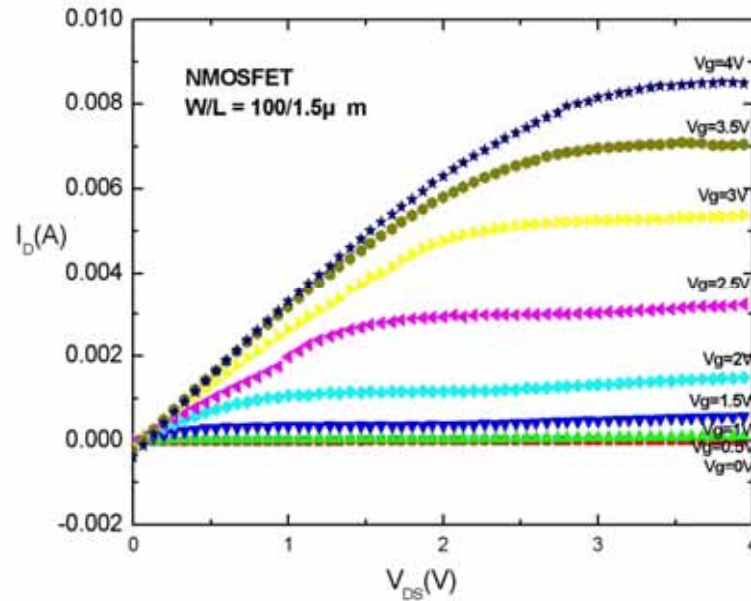


TiN / HfO₂ / Si High κ MOSFET

- A self-aligned process
- With LOCOS isolation
- HfO₂ gate dielectrics
- TiN metal gate
- 2 inch MBE-grown high κ films
- A 4 inch Si line in ERSO for isolation
- A 6 inch Si line in NDL for processing

- W / L $\sim$ 100 μ m / 1.5 μ m
- EOT $\sim$ 26 Å (t_{ox} = 10 nm)
- $I_d \sim$ 8.5 mA @ $V_{gs} = 4$ V
- $G_m = 48.5$ mS/mm





- Activation temperature: 700°C
- Transconductance G_m is increased to 48.5 mS/mm, $I_d \sim 8.5$ mA
W / L ~ 100 μm/ 1.5 μm, EOT ~ 2.6 nm.

Activation temperature (°C)	700	750	800	850
$I_D@3.5V$ (mA)	7	1.9	1.2	1.2
G_m (mS/mm)	48.5	16	12	9
L_g (μm)	1.5	2	2	2



Comparison of the High κ Transistor Results

	NTHU	Intel 2003			Intel 2004
Structure	TiN / HfO ₂ on Si	TiN / HfO ₂			TiN / HfO ₂
		Si	Strain-Si	Strain-Si	Si
L [μm]	1.5	0.14	0.14	0.08	0.08
EOT [$\text{\AA}$]	26	?	?	?	14.5
I _d [mA/mm]	85	500	625	930	1650
G _m [mS/mm]	48.5	660	750	1000	1750

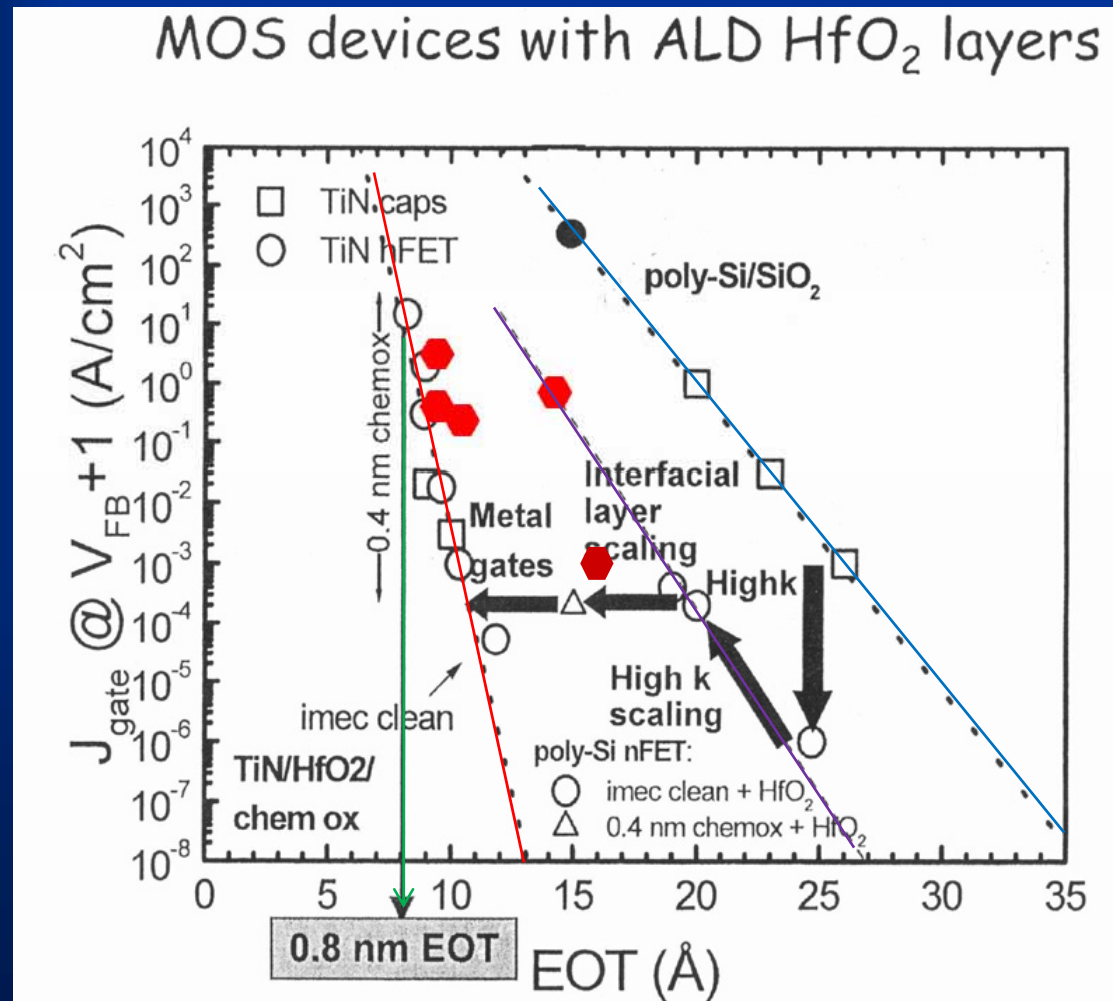
$$I_d/G_m = 50/66 \\ \text{when } L = 1.5 \mu\text{m}$$

$$I_d/G_m = 87.5/93 \\ \text{when } L = 1.5 \mu\text{m}$$

Considering the differences in L and EOT, our I_d and G_m are comparable to other leading groups.



Comparison between the MBE and ALD films



❖ MBE-grown Au/HfO₂/Si MOS diodes are denoted in red hexagons

❖ HfO₂ film 4.4 nm thick, with $J_L \sim 10^{-3} \text{ A/cm}^2$, κ of 21, an EOT of 0.9 nm

❖ $t_{\text{eq}} = \text{EOT}$
Equivalent Oxide Thickness

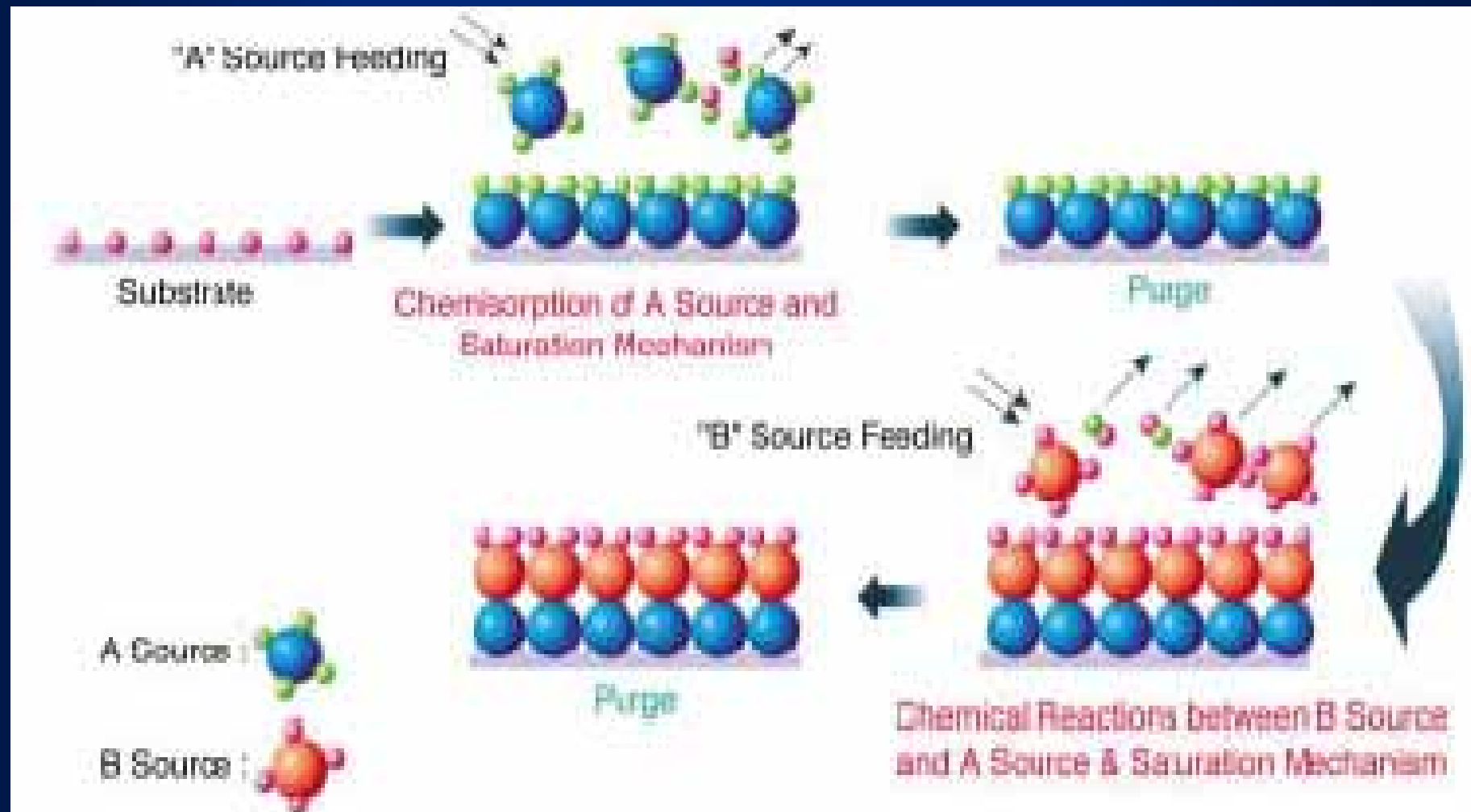
$$t_{\text{eq}} = t_{\text{ox}} \kappa_{\text{SiO}_2} / \kappa_{\text{ox}}$$

M. Houssa in Symposium D,
MRS Spring Meeting, April 12-16, 2004.



Atomic Layer Deposition (ALD)

Growth Mechanism : Formation of interfacial SiO_2 is hard to avoid.





Novel MBE template for ALD growth

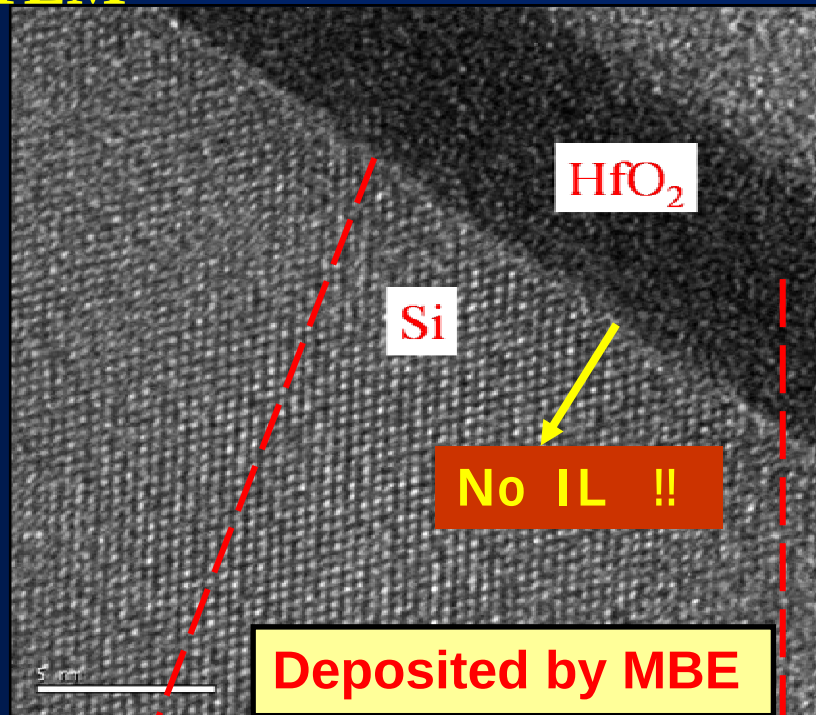
*Can you make an excellent
HfO₂ Film with a low EOT ?*

Interface Engineering !

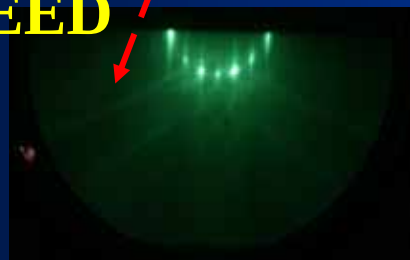


Structural properties of MBE-grown HfO_2

HRTEM



RHEED

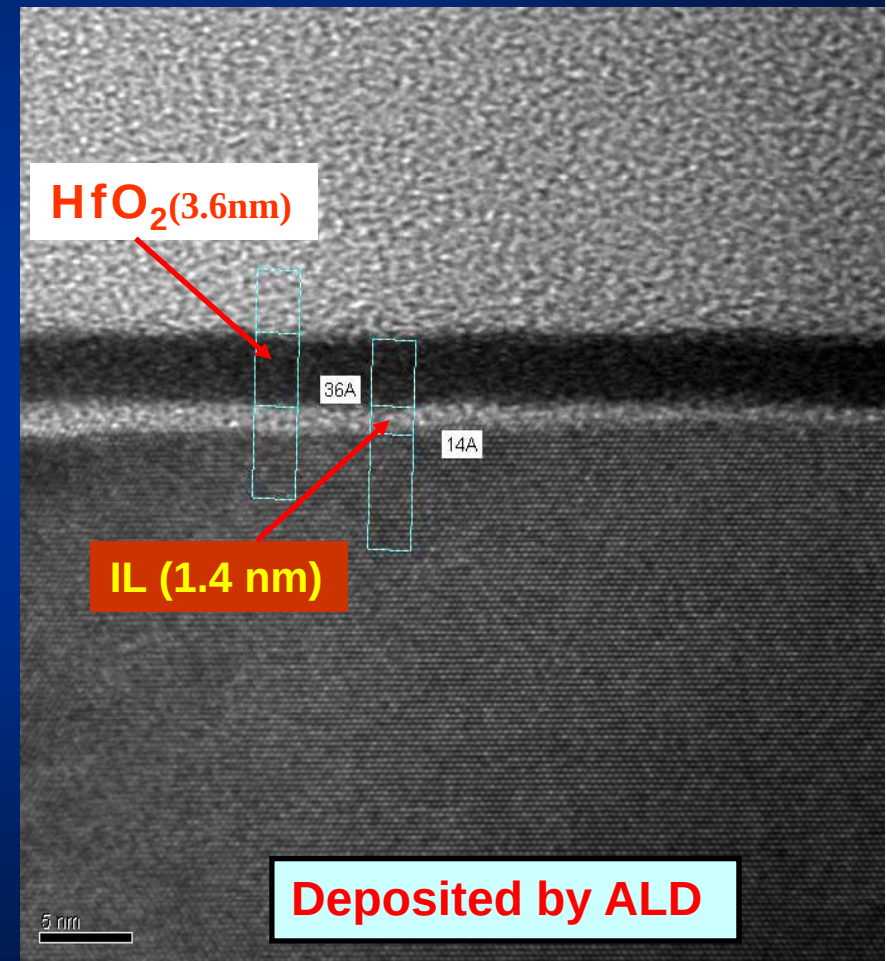


atomically order
Si(100) surface



amorphous
 HfO_2 surface

HRTEM





The MBE Template for ALD Growth

MBE and ALD composite film deposition procedure

MBE template film growth

ALD bulk film growth

MBE HfO_2

ALD HfO_2

MBE Al_2O_3

ALD Al_2O_3

Case 1

Case 2

ALD HfO_2

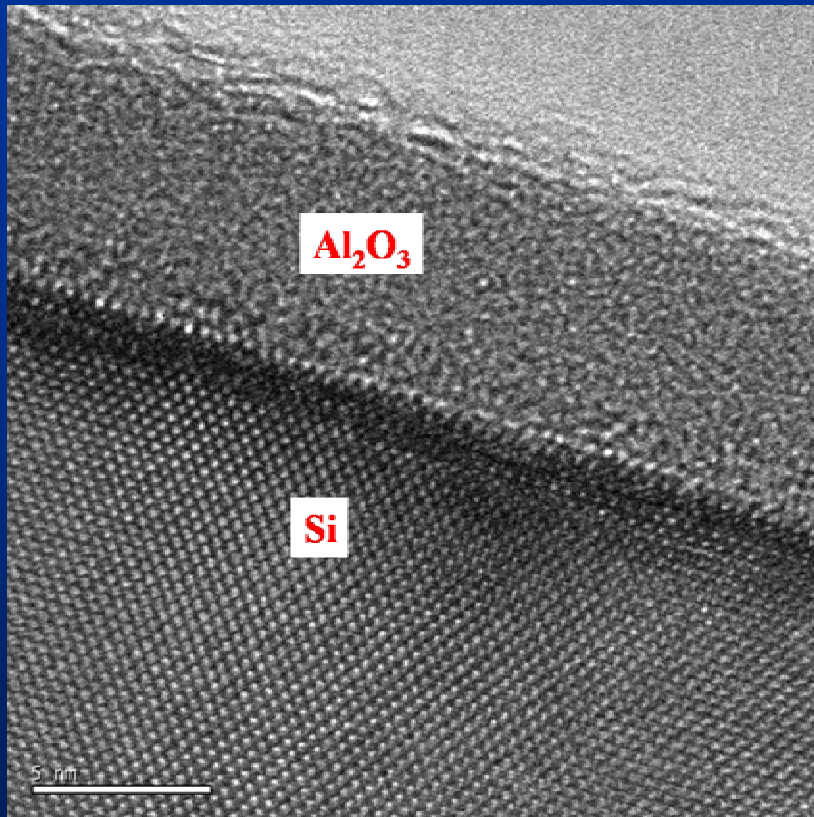
MBE HfO_2

Silicon

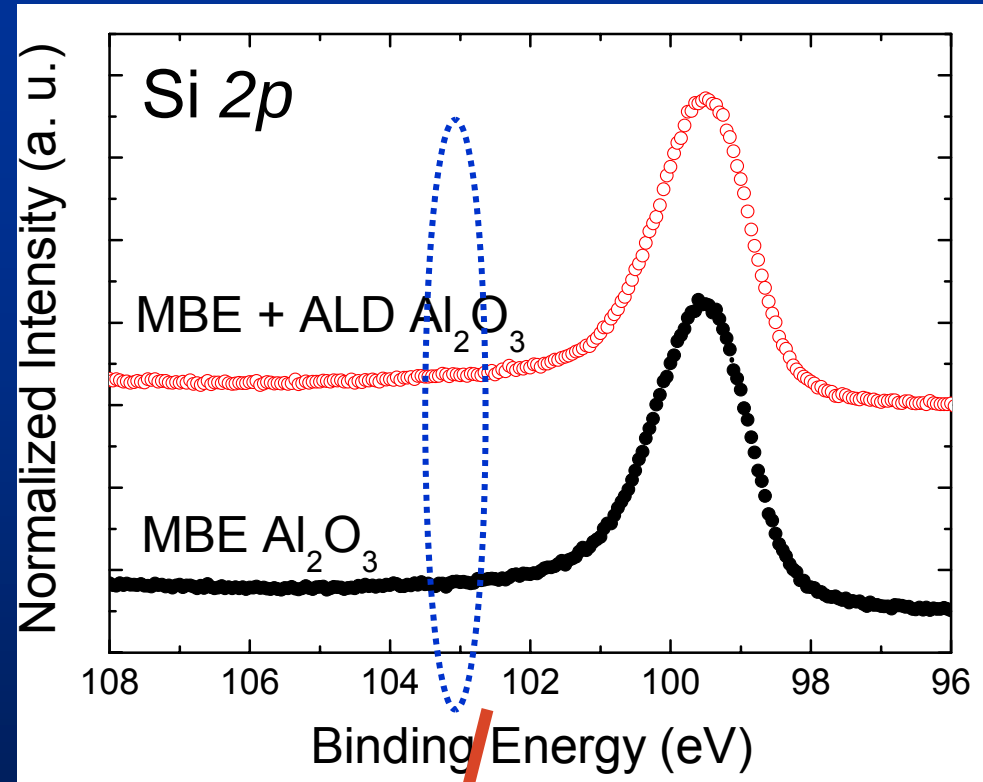
- Low pressure ($<1 \times 10^{-8}$ torr) maintained during MBE growth
- ALD precursors : TMA, H_2O , $T_{\text{substrate}}$: 300°C

The structure of ALD Al_2O_3 with a MBE Al_2O_3 template

TEM



AR-XPS



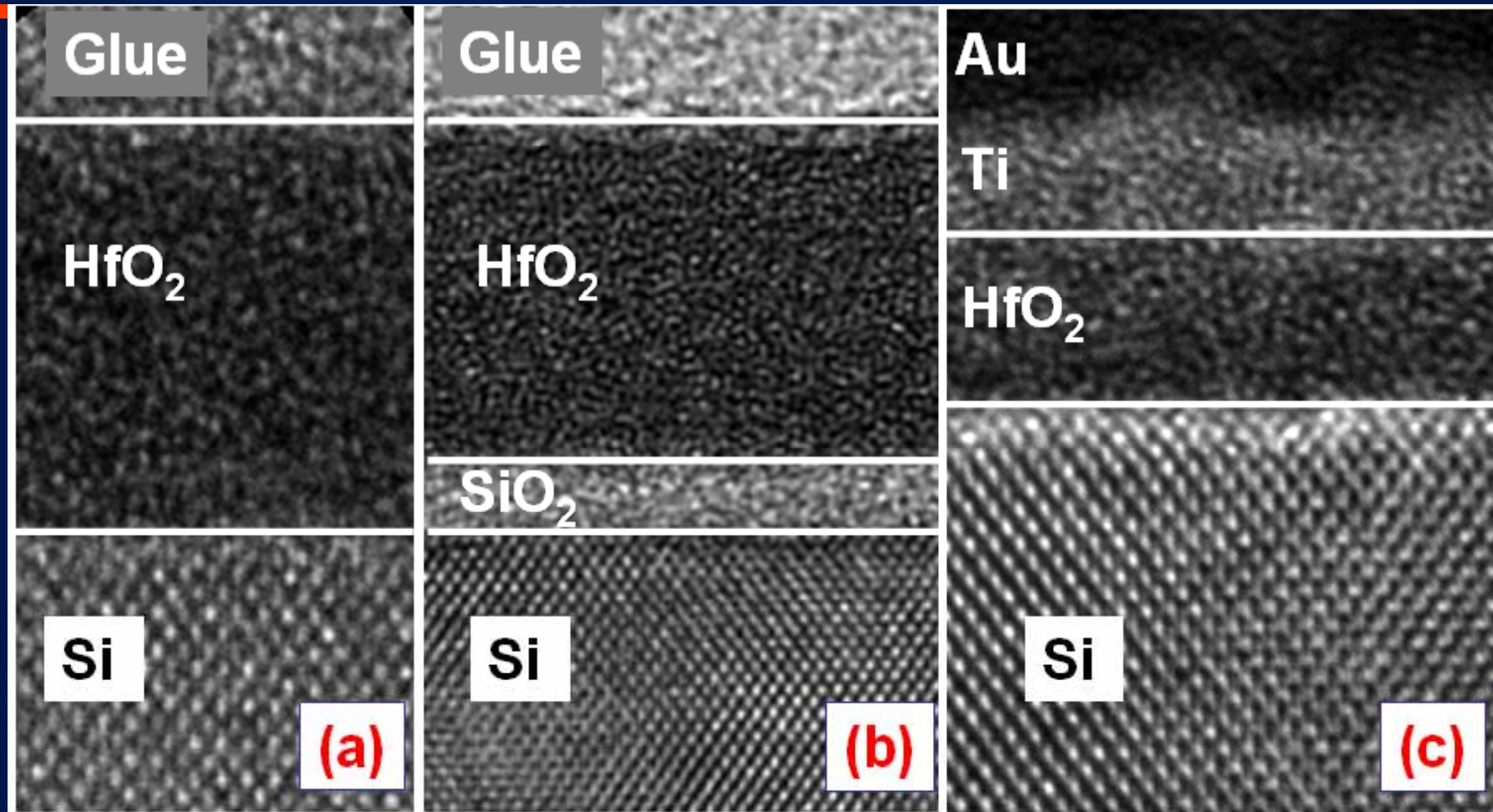
No peak formed at 103.4 eV

→ No SiO₂ formed at interface for both MBE and MBE+ALD Al₂O₃

For HfO₂, have achieved EOT= 0.7 nm



The structure of ALD HfO_2 with a MBE HfO_2 template



MBE HfO_2 (6.7nm)

Silicon

ALD HfO_2 (8.1nm)

SiO_2 (1.4nm)

Silicon

ALD HfO_2 (1.4nm)

MBE HfO_2 (1.5nm)

Silicon



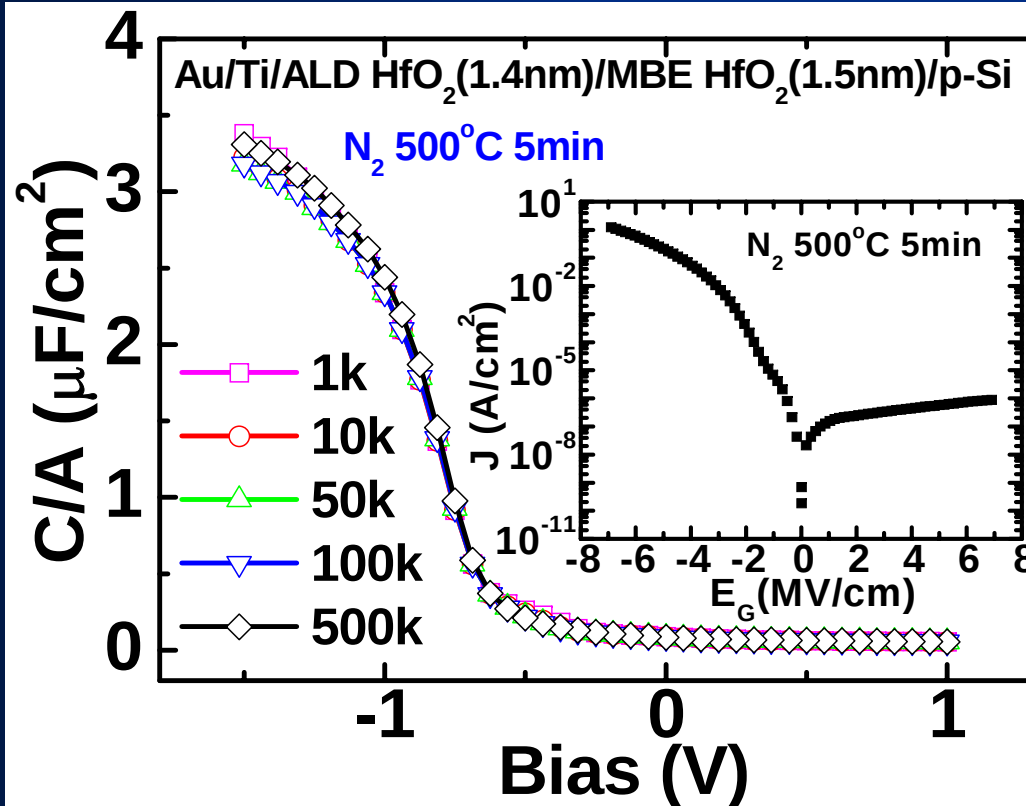
The electrical characteristics of ALD/MBE HfO₂ (2.9nm)

ALD HfO₂ (1.4nm)

MBE HfO₂ (1.5nm)

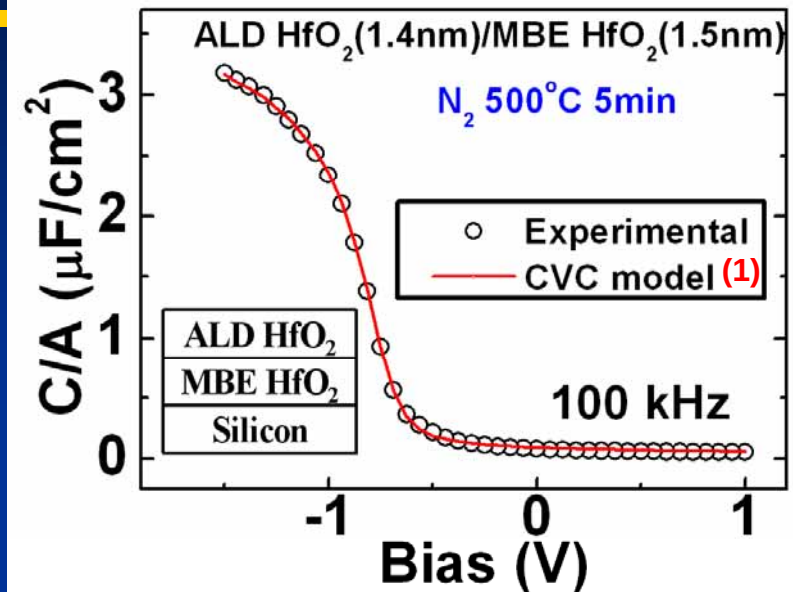
Silicon

EOT = 0.7nm

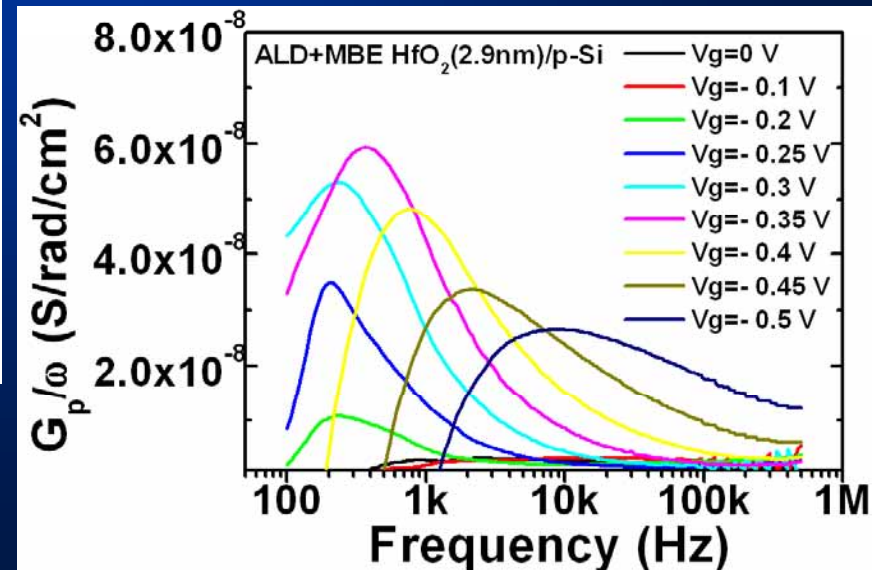


$J_{\text{leak}} = 5.3 \times 10^{-1} \text{ A}/\text{cm}^2$ at $V_{\text{FB}} - 1\text{V}$

(1) J. Hauser, CVC © 1996 NCSU software



$D_{\text{it}} = 3.6 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ near midgap





Comparisons of MOSFET Characteristics

	Our work (TiN/..../p-Si)						Intel ¹
Dielectrics	MBE-HfO ₂ 10nm	ALD-HfO ₂ 10nm	YDH 10nm	ALD-HfO ₂ 8nm+ MBE-HfO ₂ 2nm	ALD-HfO ₂ 4nm+ MBE-HfO ₂ 2nm	YDH 7nm+ Y ₂ O ₃ 1nm	ALD-HfO ₂
L _g (μm)	1.5	1.5	1.5	1	1	1	0.08
EOT(nm)	2.5	3	1.5	2.5	1.5	1.6	1
G _m (mS/mm)	35	55	70	120@V _G =3.5V 100@V _G =2.5V	<u>100@V_G=2.5V</u> 1250 [#] 1875*	<u>125@V_G=2.5V</u> 1560 [#] 2500*	132 1650
I _d (mA/mm)	80	55	118	240@V _G =4V 70@V _G =2.5V	<u>155@V_G=2.5V</u> 1940 [#] 2910*	<u>195@V_G=2.5V</u> 2440 [#] 3900*	140 ¹ 1750

After normalization to gate length of 0.08 μm

* After normalization to gate length of 0.08 μm and EOT of 1 nm

¹ R. Chau, et al, IEEE Electron Device Letters **25**, No. 6, 408 (2004)



Major Research Accomplishment

- First demonstration of atomically abrupt high k HfO_2/Si interface.
- Successful integration of the 6 inch Si CMOSFET processing in NDL with our 2" MBE high κ dielectric films using a TiN metal gate to produce a gate length 1.5 μm transistor device.
- Novel ALD + MBE template approach, superior electrical performance.

