Nanoelectronics on Si

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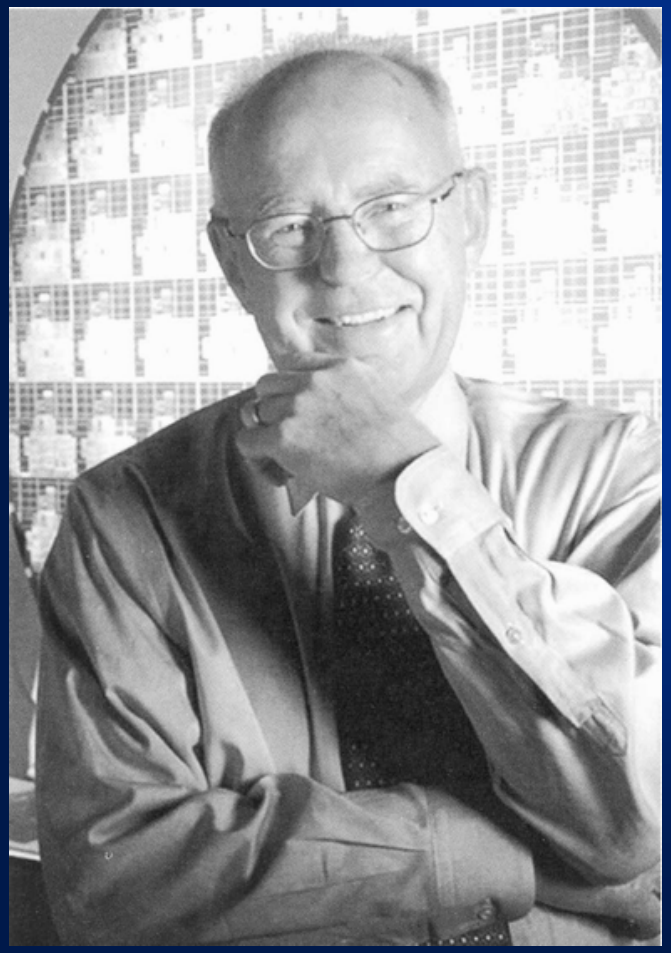
近年奈米科技之發展

- 縮小尺度至100 nm以內的科技：
  Top-down之奈米結構的雕刻細化
  莫爾定律(Moore's law－每1.5年縮小30%尺寸)

- 操控原子（分子）的科技：Bottom-up 之奈米體系的成長組裝
  費曼的主張－從底部作起，下面還有無限寬廣的空間

近來大力推動奈米科技的背景

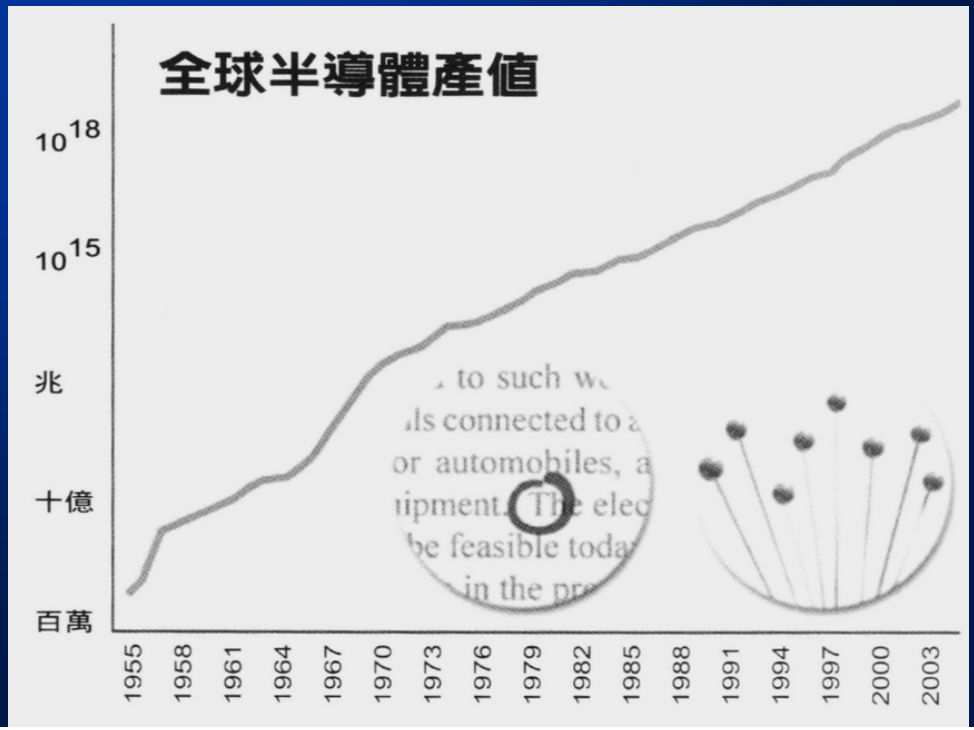
來自微電子學可能遭遇瓶頸的考慮



Moore‘s Law： 摩爾定律

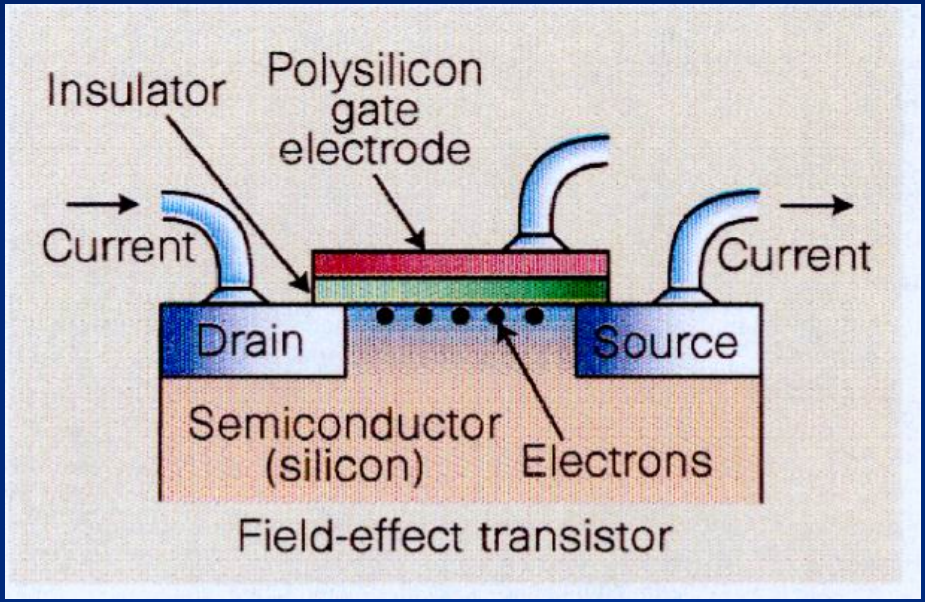
A 30% decrease in the size of printed dimensions every 1.5 years.

矽晶上電子原件數每1年半會增加一倍



Device Scaling, Moore's Law

1960 Kahng and Atalla, First MOSFET



Moore's Law:

The number of transistors per square inch doubles every 18 months

Shorter gate length L

Thinner gate dielectrics t_{ox}

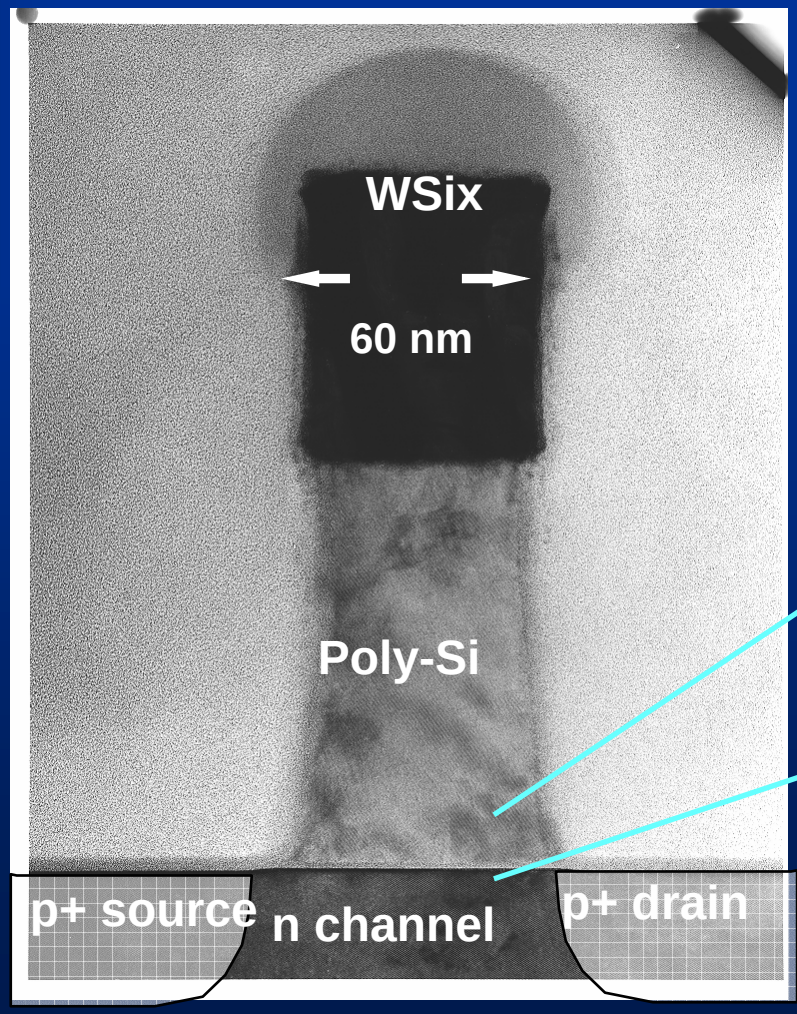
Driving force :

High speed

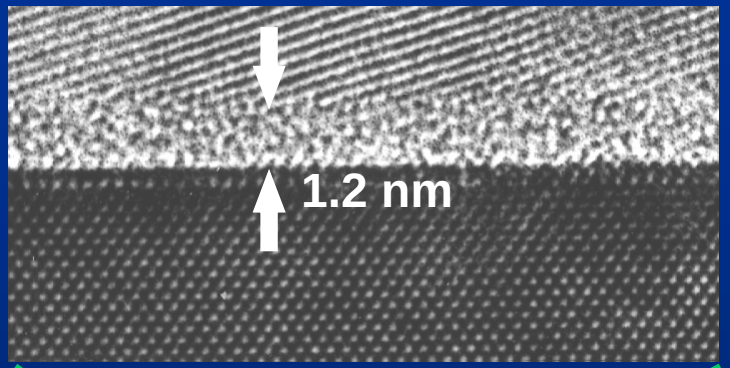
Lower power consumption

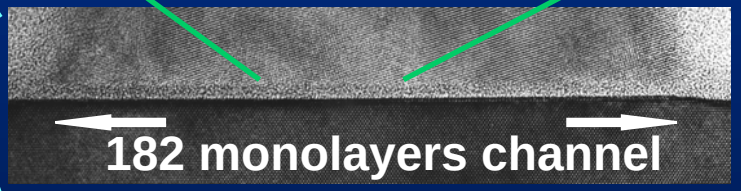
High package density

Scaling Limits to CMOS Technology



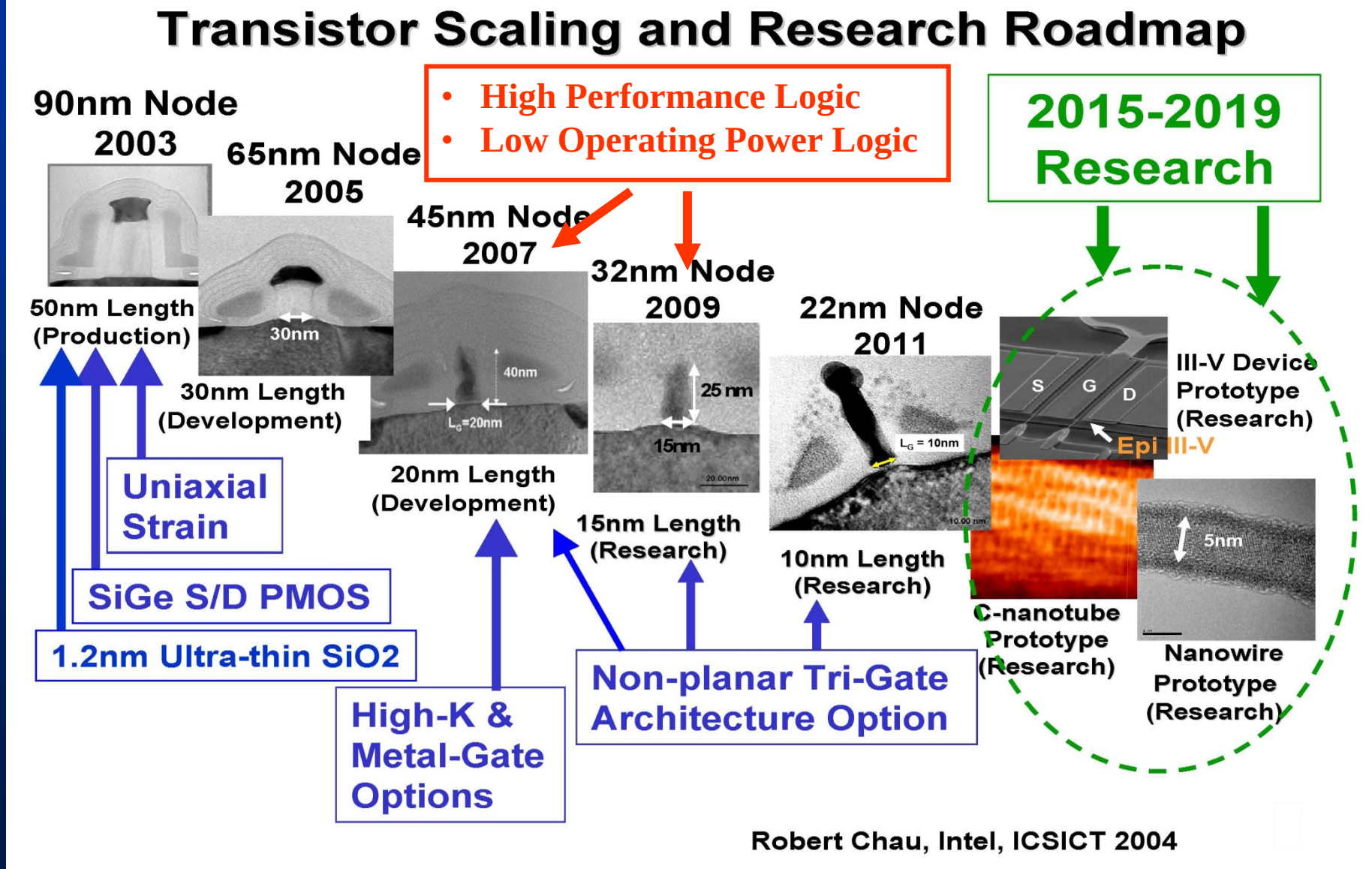
Gate Oxide ~ 5 Si Atoms thick !





Shrinking the junction depth ➡ increasing the carrier concentration

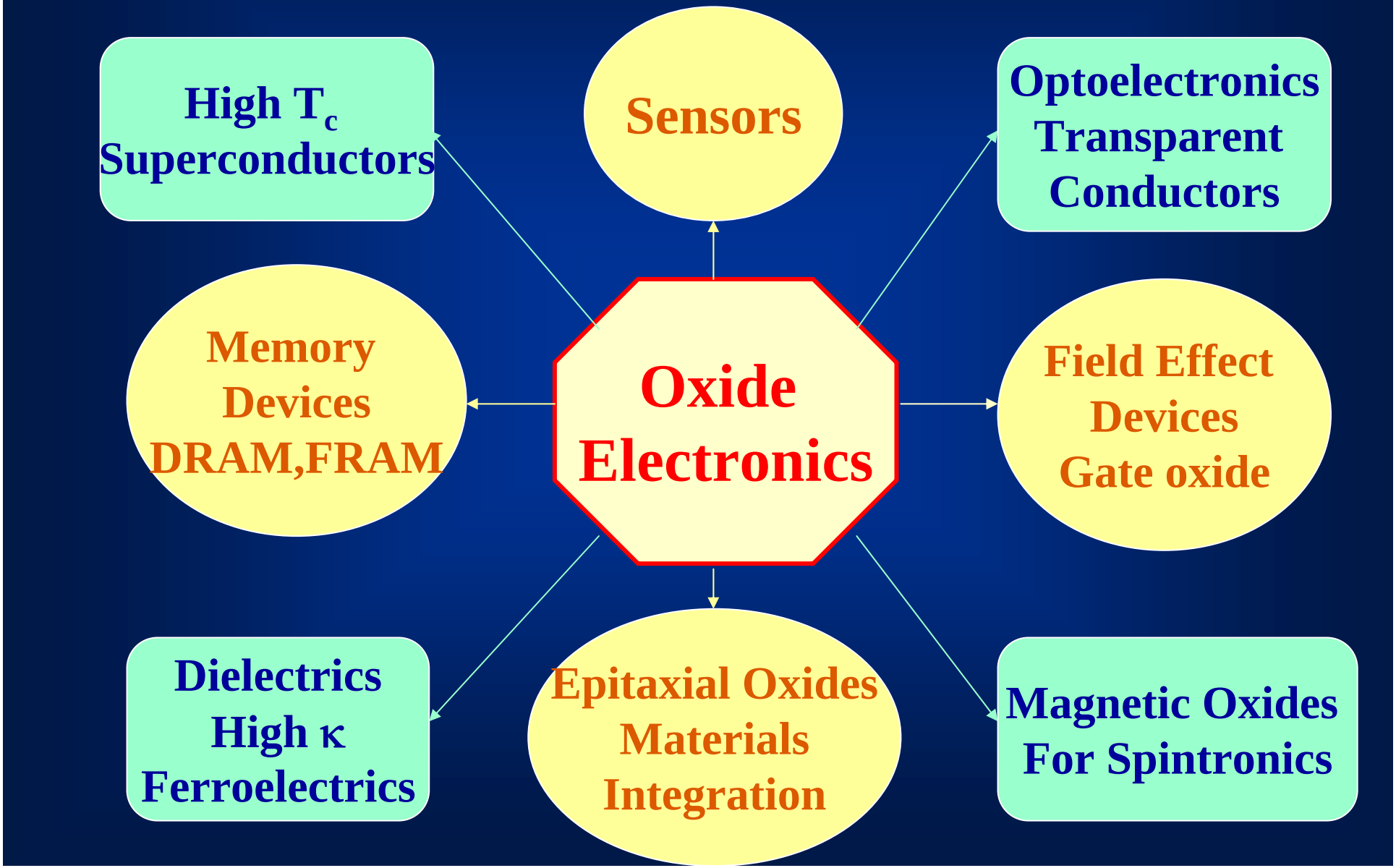
Intel Transistor Scaling and Research Roadmap



TALK OUTLINES

- The alternative high κ gate dielectrics replacing SiO_2 for 33 nm Si CMOS by year 2009
  - -- Materials requirements
  - -- Processing integration issues
- MBE grown HfO_2 high κ gate dielectrics
  - -- thermal stability studies by MEIS and TEM
  - -- electrical performance
- Integration of ALD + MBE template approach

The Development of Oxide Electronics in Two Decades



CMOS scaling, When do we stop ?

Reliability: 25 ~~22~~ ~~18~~ ~~16~~ Å

processing and yield issue

Tunneling : 15 Å

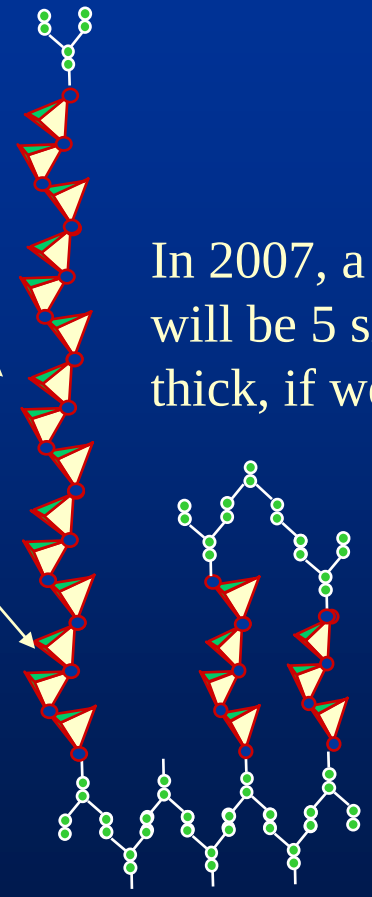
Design Issue: chosen for 1A/cm^2 leakage
I_{on}/I_{off} >> 1 at 12 Å

Bonding:

Fundamental Issues---

- how many atoms do we need to get bulk-like properties?
  EELS -- Minimal 4 atomic layers !!
- Is the interface electronically abrupt?
- Can we control roughness?

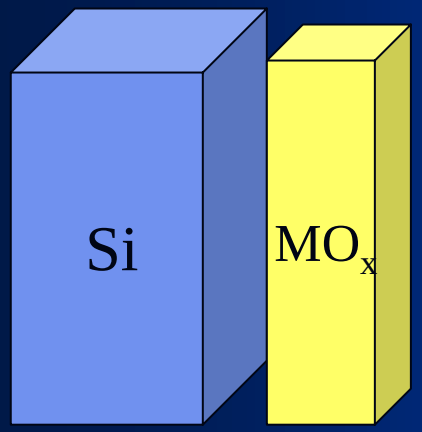
In 1997, a gate oxide was 25 silicon atoms thick.



In 2007, a gate oxide will be 5 silicon atoms thick, if we still use SiO_2

and at least 2 of those 5 atoms will be at the interfaces.

Fundamental Materials Selection Guidelines



$Si + MO_x \longrightarrow M + SiO_2$

$Si + MO_x \longrightarrow MSi_2 + SiO_2$

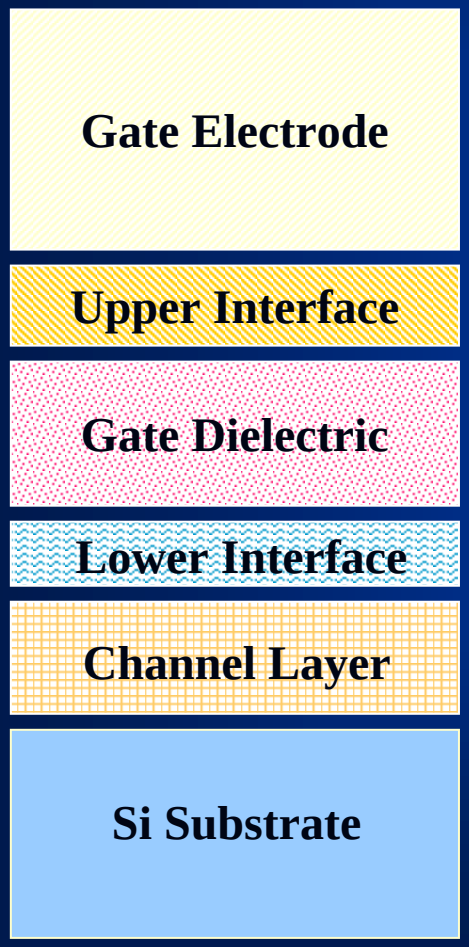
$Si + MO_x \longrightarrow MSiO_x + SiO_2$

- Thermodynamic stability in contact with Si to 750ºC and higher. **(Hubbard and Schlom)** **Alkaline earth oxide, IIIB, IVB oxide and rare earth oxide**
- Dielectric constant, band gap, and conduction band offset
- Defect related leakage, substantially less than SiO_2 at $t_{eq} < 1.5$ nm
- Low interfacial state density $D_{it} < 10^{11}\ eV^{-1}cm^{-2}$
- Low oxygen diffusivity
- Crystallization temperature >1000°C

t_{eq} : **equivalent oxide thickness (EOT) to be under 1.0 nm**

$t_{eq} = t_{ox}\ \kappa_{SiO2} / \kappa_{ox}$

Integration Issues for High κ Gate Stack



Critical Integration Issues

- Morphology dependence of leakage
  Amorphous vs crystalline films?
- Interfacial structures
- Thermal stability
- Gate electrode compatibility
- Reliability

Fundamental Limitations

- Fixed charge
- Dopant depletion in poly-Si gate
- Dopant diffusion
- Increasing field in the channel region

Basic Characteristics of Binary Oxide Dielectrics

Dielectrics	SiO_2	Al_2O_3	Y_2O_3	HfO_2	Ta_2O_5	ZrO_2	La_2O_3	TiO_2
Dielectric constant	3.9	9.0	18	**20**	25	27	30	80
Band gap (eV) Band offset (eV)	9.0 3.2	8.8 2.5	5.5 2.3	**5.7** **1.5**	4.5 1.0	7.8 1.4	4.3 2.3	3.0 1.2
Free energy of formation $MO_x+Si_2 \rightarrow M+ SiO_2$ @727C, Kcal/mole of MO_x	-	63.4	116.8	**47.6**	-52.5	42.3	98.5	7.5
Stability of amorphous phase	High	High	High	**Low**	Low	Low	High	High
Silicide formation ?	-	Yes	Yes	**Yes**	Yes	Yes	Yes	Yes
Hydroxide formation ?	-	Some	Yes	**Some**	Some	Some	Yes	Some
Oxygen diffusivity @950C (cm^2/sec)	$2x\ 10^{-14}$	$5x\ 10^{-25}$	?	**?**	?	10^{-12}	?	10^{-13}

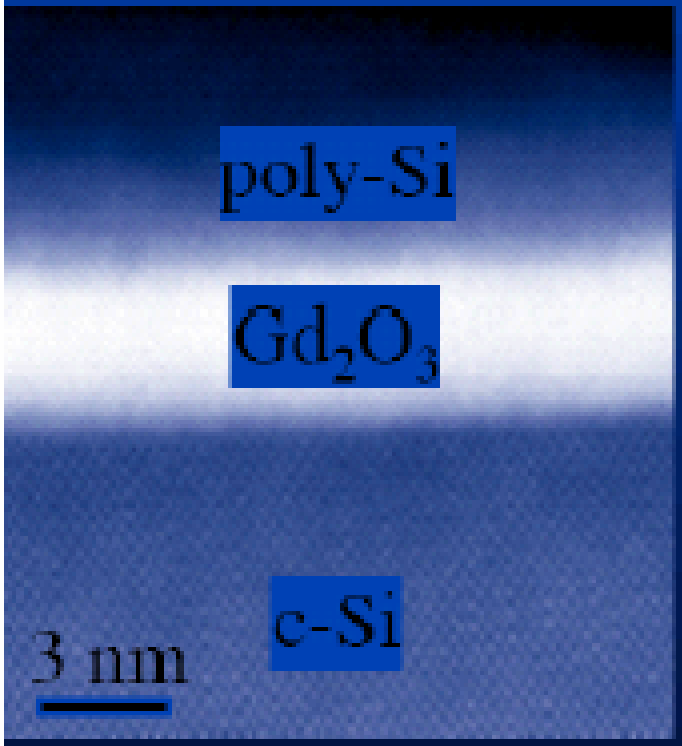
Assessing Thermodynamic Stability

Gate Dielectric Material

Silicon

Ideal "Gedanken" Interface

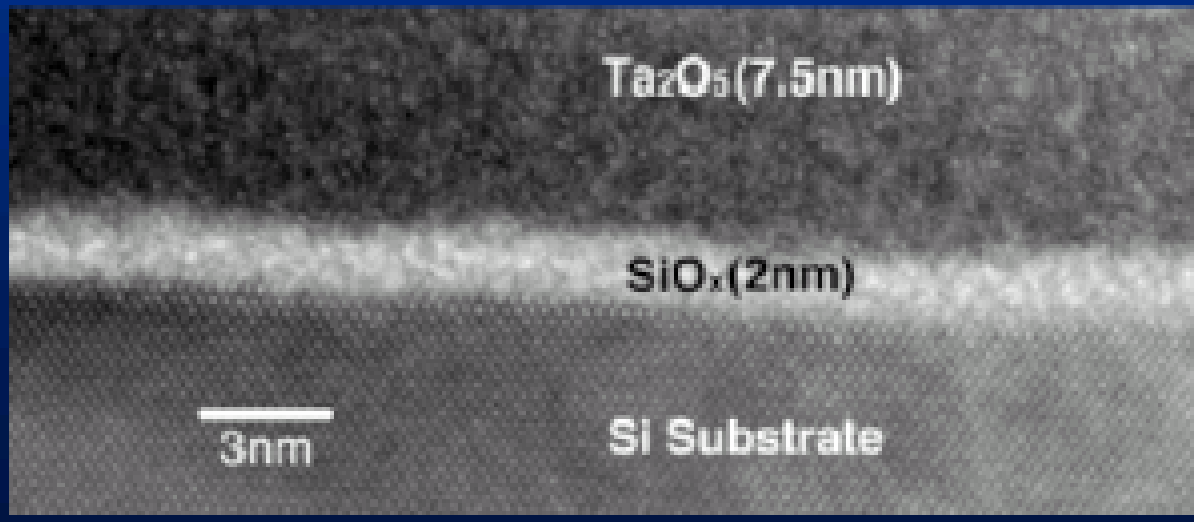
Stable Interface



TEM by David A. Muller

J. Kwo *et al.*, J. Appl. Phys. 89 (2001) 3920.

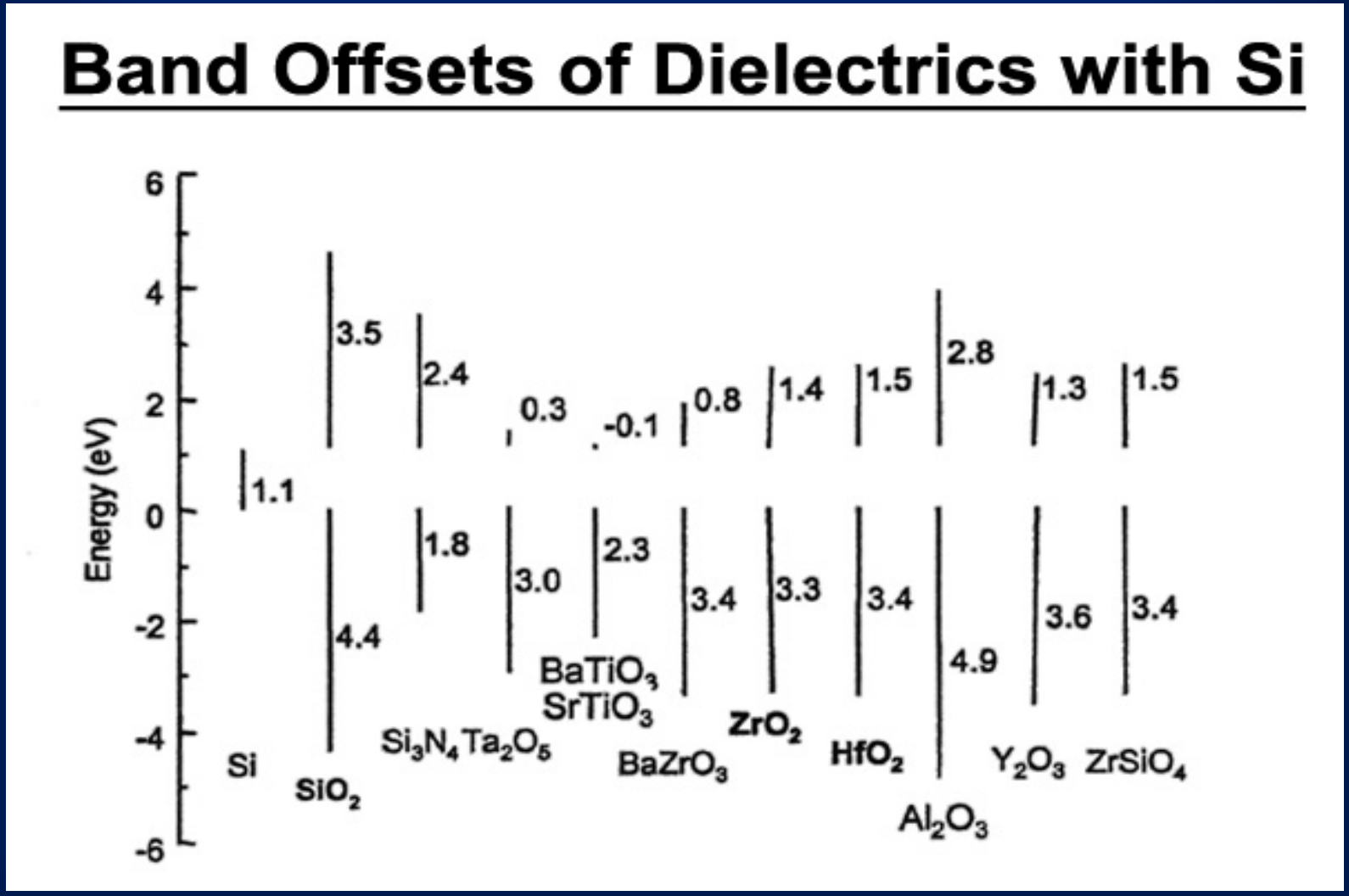
Unstable Interface



TEM by Don J. Werder

G.B. Alers *et al.*, Appl. Phys. Lett. 73 (1998) 1517.

Band Offset of High κ Dielectrics



J. Roberson, JVST 18, 1785, (2000)

A Topic Well Worth Doing Research On !!!

World production in year 2003: 1×10^{19} transistors

World population: 6.4×10^{9} people

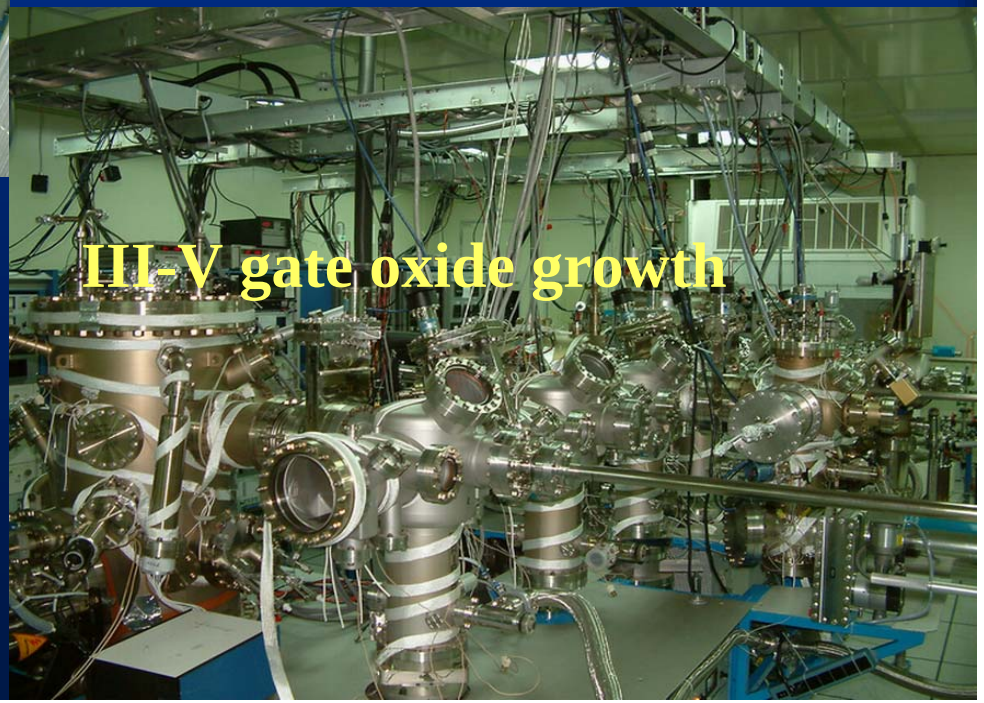
So, the world produces:

- ~ 1.5×10^{9} transistors/person each year
- ~ 1.2×10^{8} transistors/person each month
- ~ 4M transistors/person each day
- ~ 3K transistors/person each minute
- ~ 50 transistors/person per second

And Taiwan produces ~5000 transistors/person/per second

MBE Integrated Multi-chamber System For Nano Electronics

Si gate oxide growth

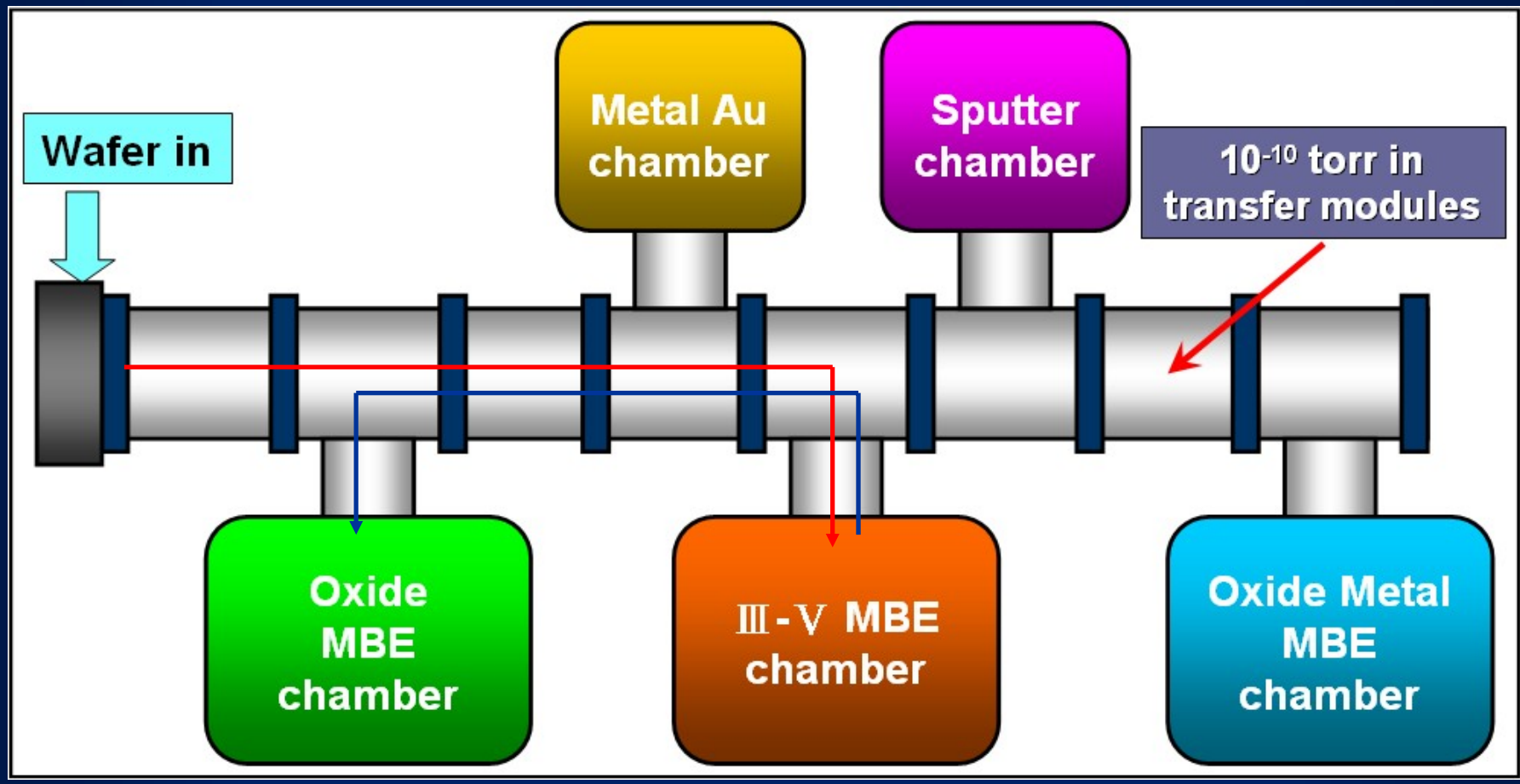


III-V gate oxide growth

Now located in the Nano Technology Center, ITRI, Hsin Chu, Taiwan since 7/2003.

In-situ Fabrication

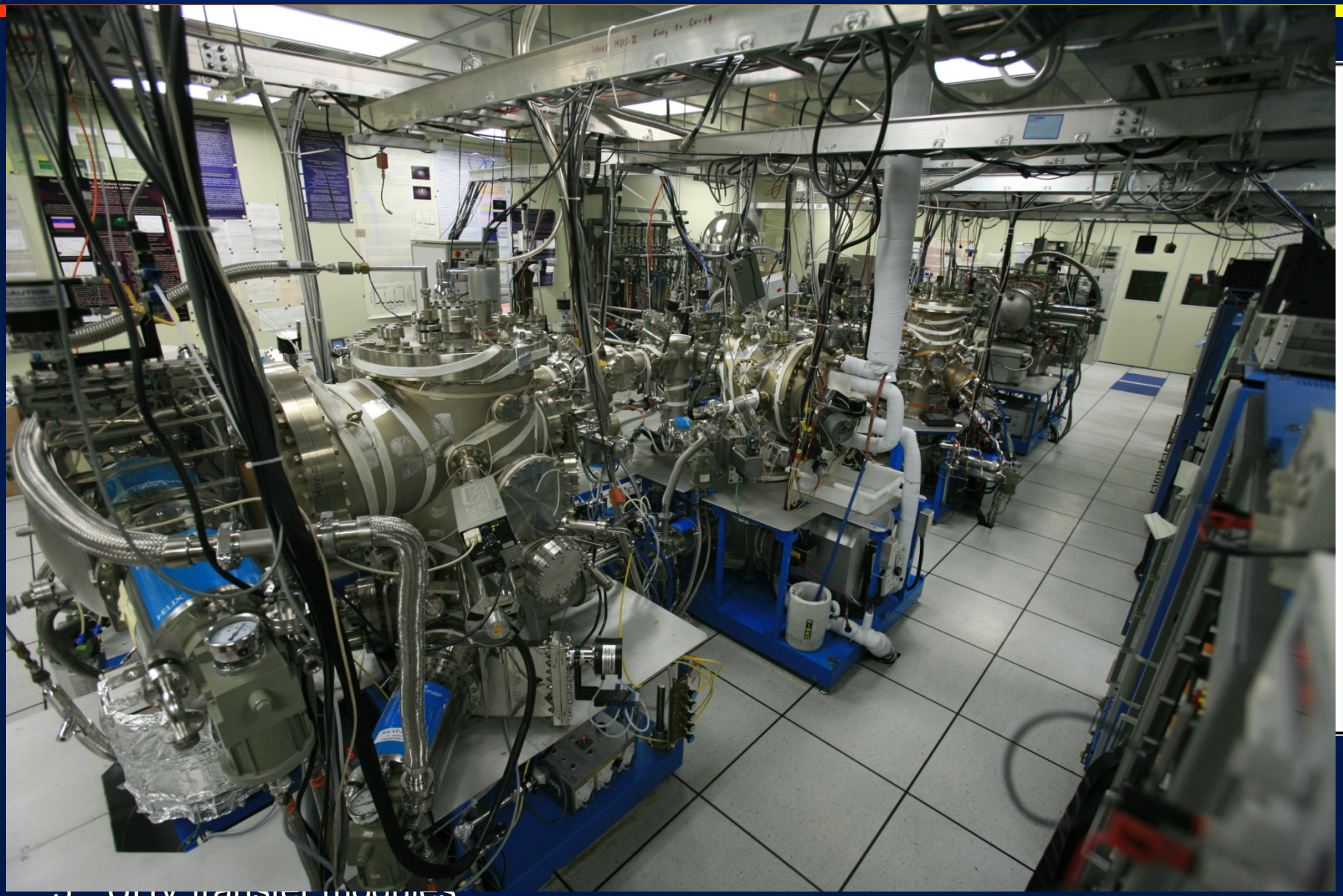
UHV integrated processing system



Multichamber Ultrahigh Vacuum System

1. A solid source GaAs-based MBE chamber
2. Oxide deposition chamber (As-free)
3. UHV transfer modules

In-situ Fabrication



5. UHV transfer modules

High κ Dielectrics for Si

- Epitaxial crystalline films on Si

  (A) Cubic CaF_2 structure:

  (111) orientation is more common than (100)

  e.g. CaF_2 (111), CeO_2 (111) on Si(111) with ε ~ 26

  YSZ (100) on Si(100) with ε~ 25-30

  (B) Cubic Mn_2O_3 structure

  ~ 8 unit cells of incomplete fluorite structure

  e.g. Y_2O_3 (110) on Si(100) with ε ~ 16-18

  Gd_2O_3 (110) on Si(100) with ε ~ 12-14

  (C) Ternary perovskite structure

  e.g. $SrTiO_3$ (100) on Si(100) with ε~ 70-80 (Oakridge, Motorola)

  using a Sr silcide ¼ monolayer for epi-growth

- Amorphous oxide films on Si

  e.g. Si_3N_4, Al_2O_3, Ta_2O_5, ZrTiSnOx, TiO_2 Interfacial layer present

  - Amorphous Gd_2O_3 and Y_2O_3 films

  - Amorphous SiO_2 added with Hf or Zr . (G. Wilks et al)

Research Programs

- Low defect high κ ultrathin films
  --Interface engineering
  --Electrical characterization and optimization

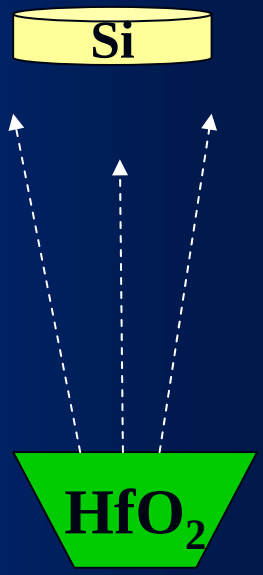
- Identify new material candidates for metal gate
  --Metal gate/high κ integration

- Integration of high κ, and metal gate with Si- Ge strained layer
  Integration of high κ, and metal gate with strained Si

- High k dielectrics for high mobility III-V semiconductors

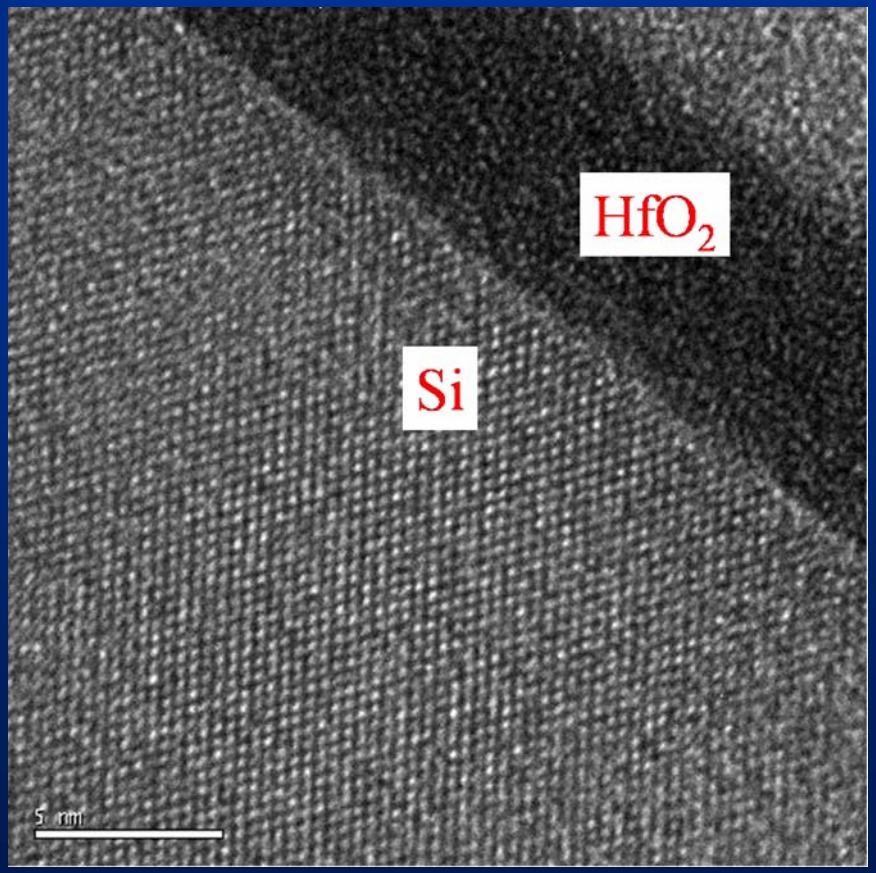
MBE Growth of High κ Oxides

- Ultrahigh vacuum, multi-chamber MBE system.
- Electron-beam evaporation of oxide sources from pressed ceramic pellets.
- 2 inch RCA-cleaned Si wafers, hydrogen passivated, followed by prompt insertion into UHV.
- In-situ heating to 400-500C to attain a (2 x 1) reconstructed Si surface.
- Substrate temperature of 550C for **epitaxial** films.
- Room temperature deposition for **amorphous** films.
- Maintain **low pressure** during growth < 1.0×10^{-9} torr.



High Resolution Cross Sectional TEM and RHEED Images of HfO_2 on Si (100)

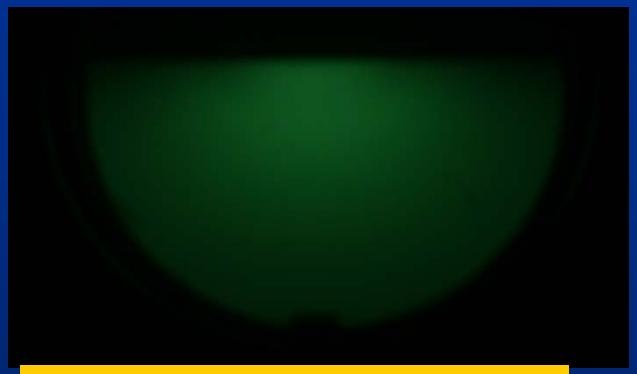
From AFM: RMS Roughness: 0.072nm



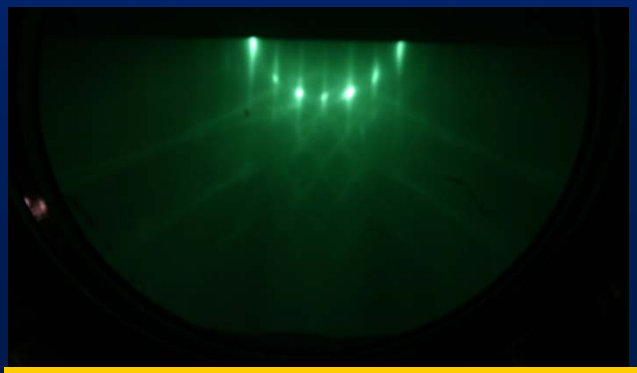
Amorphous HfO_2 film 6.0 nm

SiO_2 and Hf silica is nearly absent !

RHEED

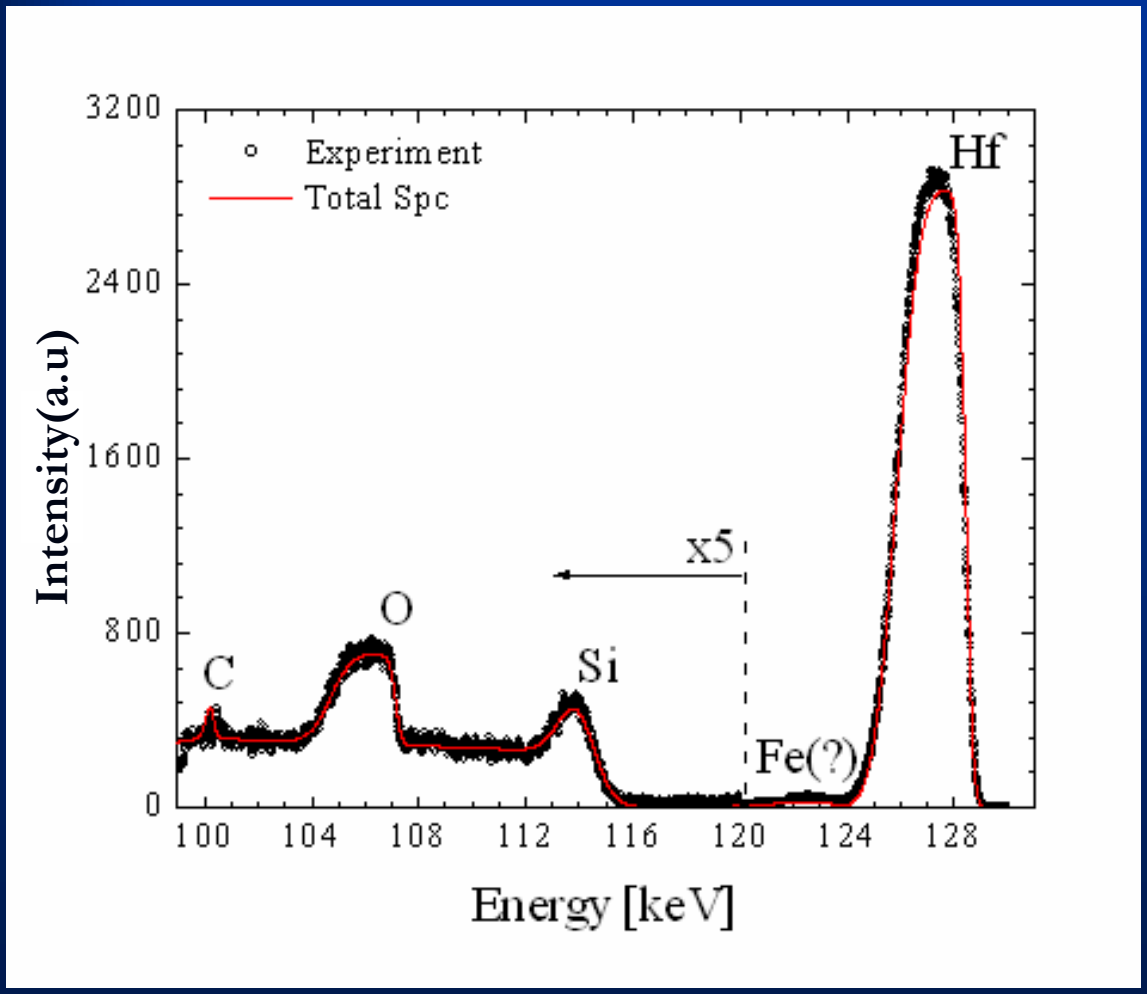


amorphous HfO_2 surface



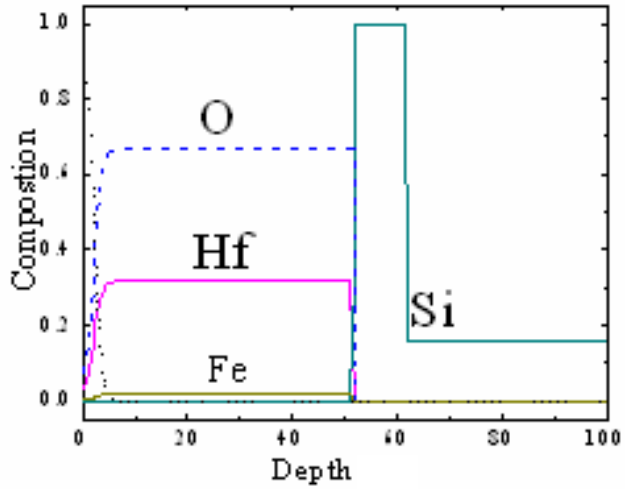
atomically order Si(100) surface

Medium Energy Ion Scattering (MEIS) Study of the High κ Dielectric / Si Interface and Stability



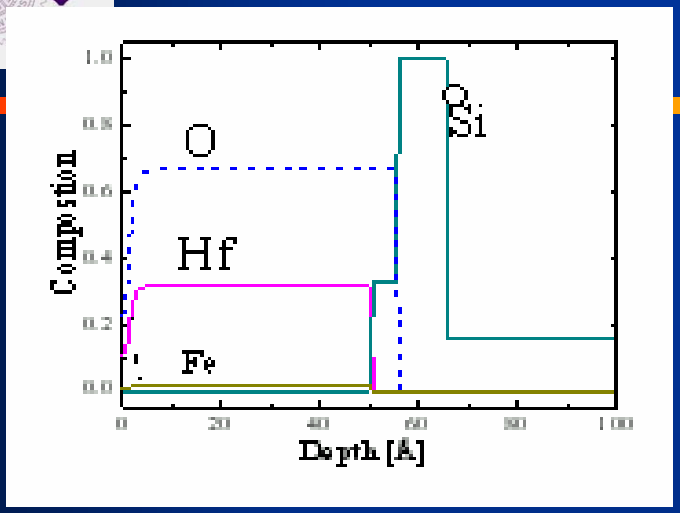
HfO_2 50 Å

Si(100)

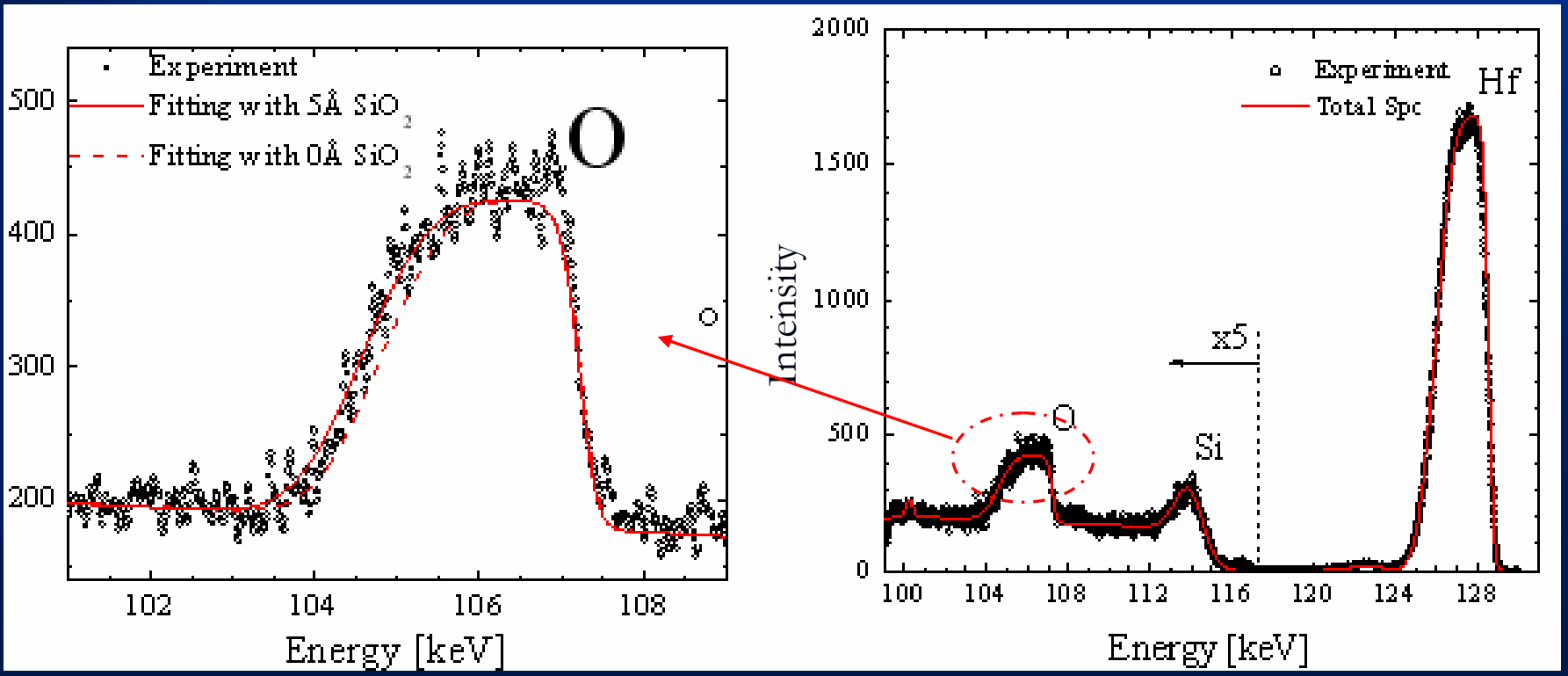


With Rutgers University using 130 keV proton beam
It shows the absence of silica near the interface.

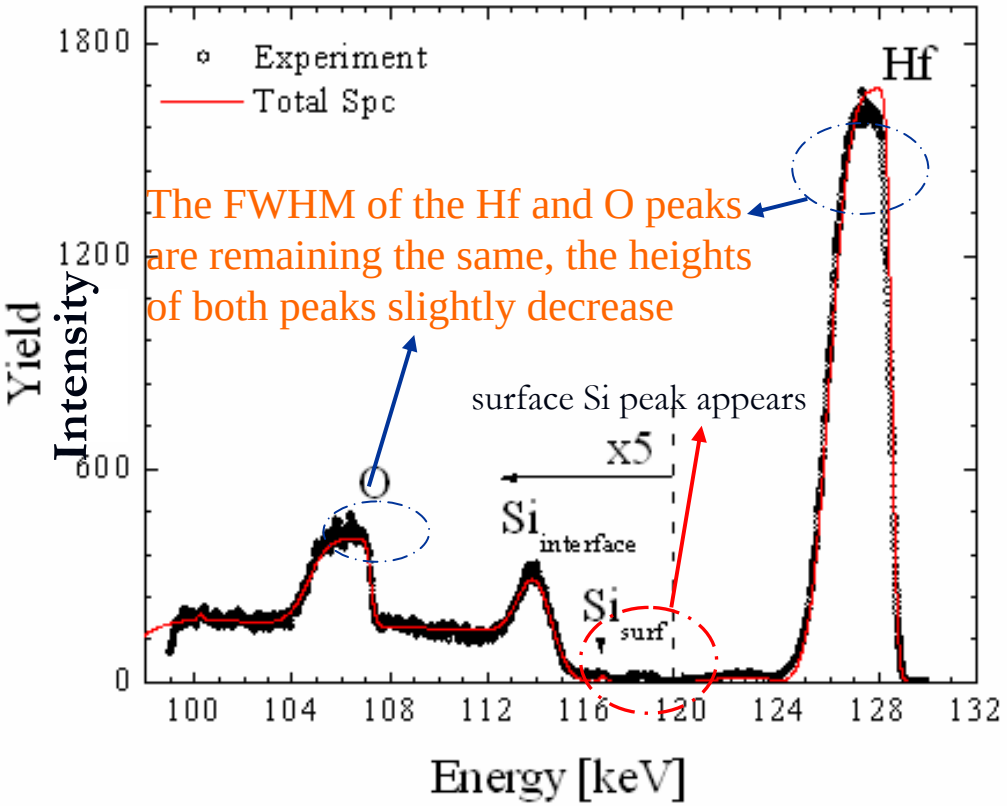
Vacuum annealing at 630°C



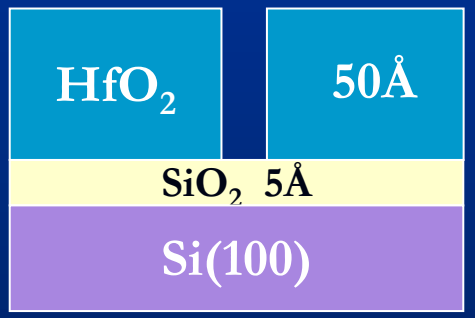
Broadening of the O peak and small increase in the Si peak indicate some interfacial SiO_2 formation about 0.4 nm.



Annealing from 630°C to 950°C



A possible structure after high temperature anneal

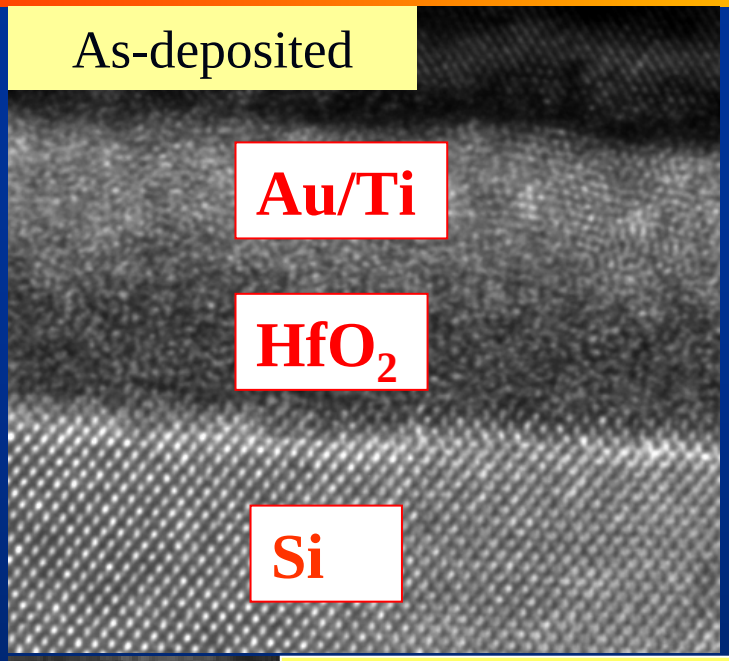


Discontinuities and islands were formed in HfO_2 .

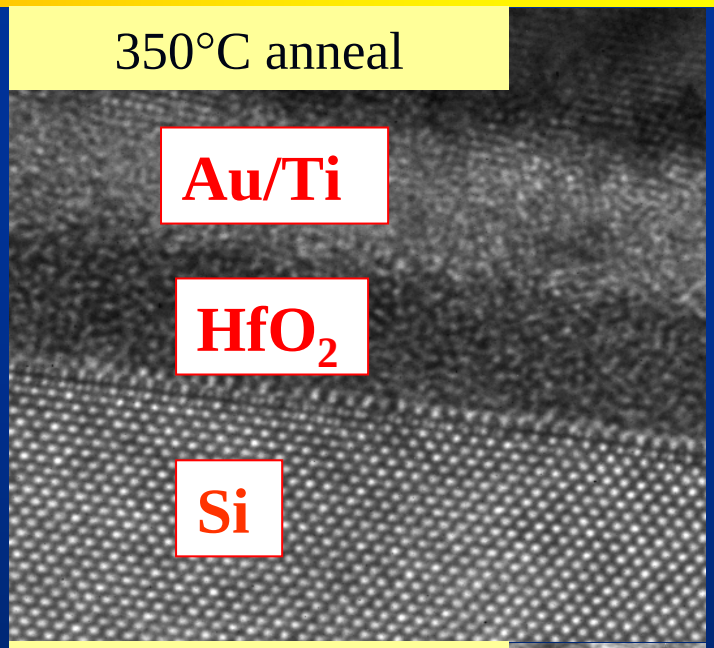
MEIS with Rutgers University

HRTEM Study of Thermal Stability of High κ HfO_2 Gate Stacks

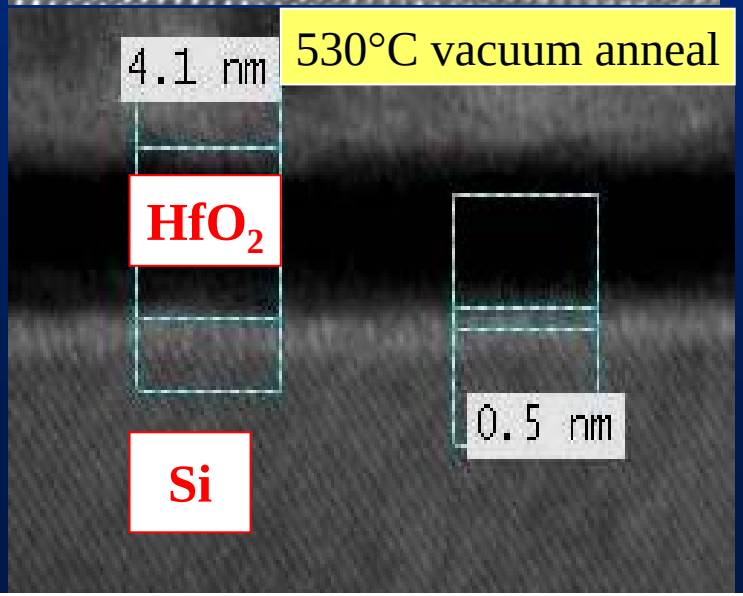
As-deposited



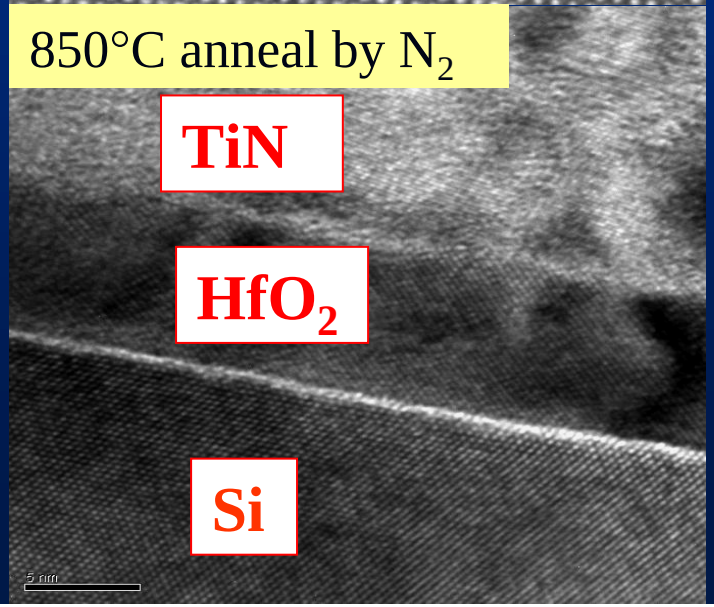
350°C anneal



530°C vacuum anneal



850°C anneal by N_2



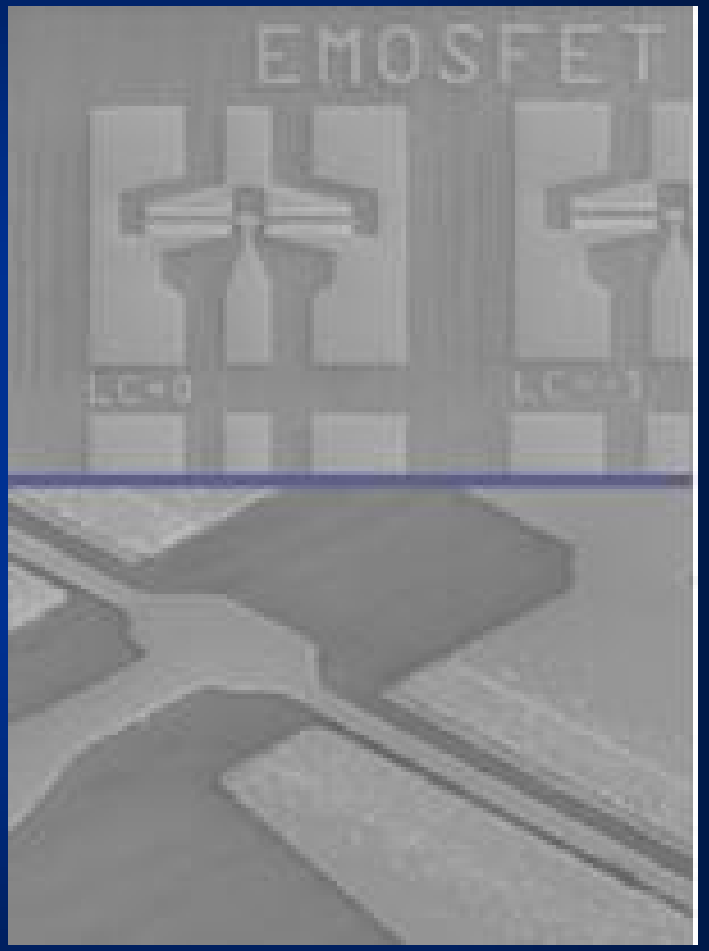
Difficulties of High κ MOSFET Fabrications

- Thermal stability of thin films
  - HfO_2 → Lowering the dopant activation temperature to 700°C
  - TiN → Using Ti/TiN bilayer structure
- Process integration
  - 4 inch Si (LOCOS)→2 inch Si (MBE)

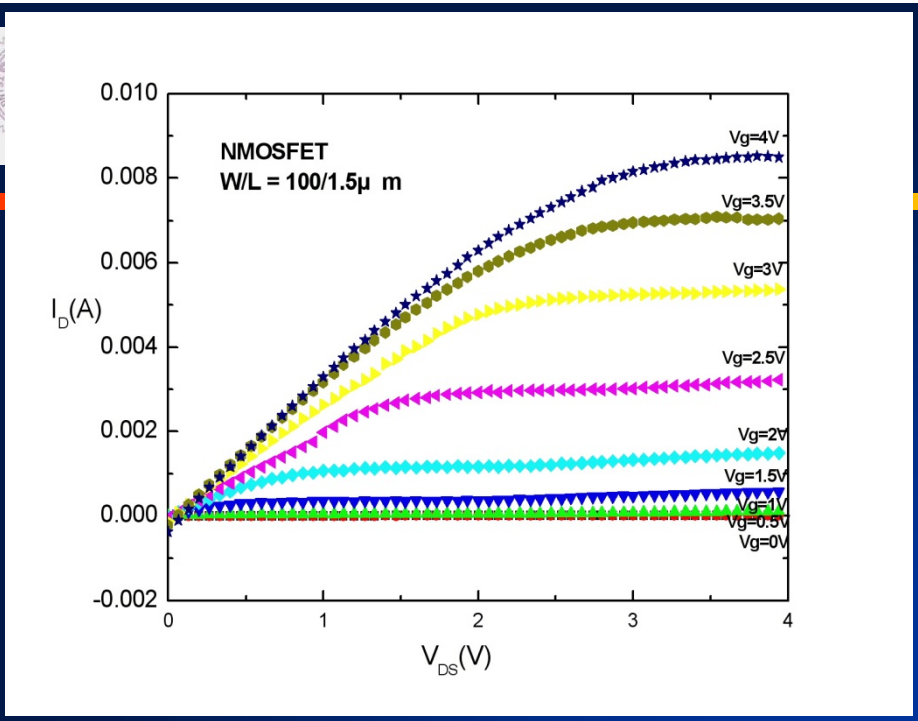
→ Successful integration

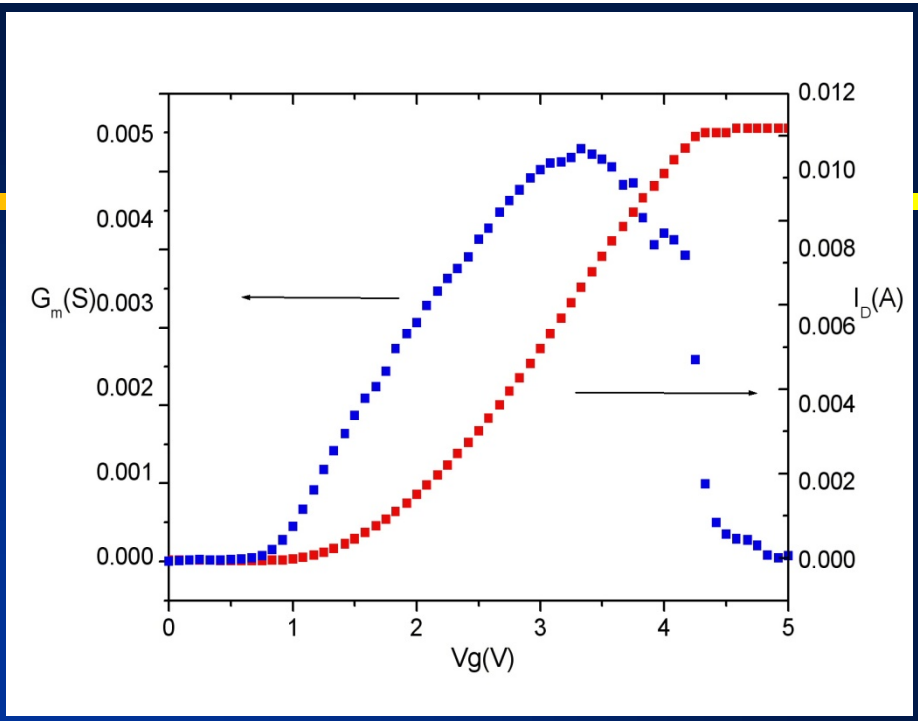
TiN/HfO_2/Si High κ MOSFET

- A self-sligned process
- With LOCOS isolation
- HfO_2 gate dielectrics
- TiN metal gate
- 2 inch MBE-grown high κ films
- A 4 inch Si line in ERSO for isolation
- A 6 inch Si line in NDL for processing



- W / L ~ 100 μm/ 1.5 μm
- EOT ~ 26 A (t_{ox} = 10 nm)
- I_d ~ 8.5 mA @ V_{gs} = 4V
- Gm = 48.5 mS/mm





- Activation temperature: 700°C
- Transconductance G_m is increased to 48.5 mS/mm, I_d ~ 8.5 mA W / L ~ 100 μm/ 1.5 μm, EOT ~ 2.6 nm.

Activation temperature (°C)	700	750	800	850
I_D@3.5V (mA)	7	1.9	1.2	1.2
G_m (mS/mm)	48.5	16	12	9
L_g (μm)	1.5	2	2	2

Comparison of the High κ Transistor Results

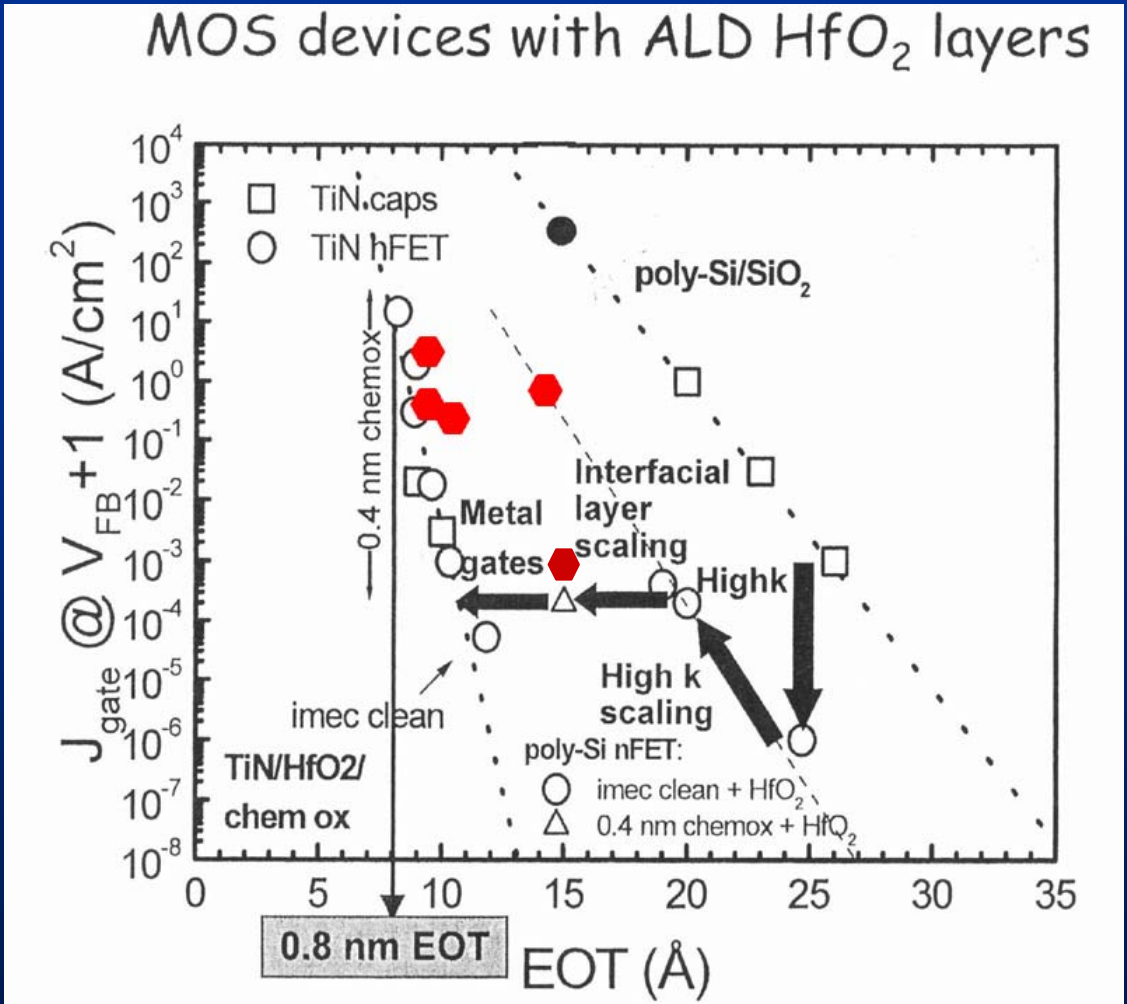
	NTHU	Intel 2003			Intel 2004
Structure	TiN/HfO_2 on Si	TiN/HfO_2			TiN/HfO_2
		Si	Strain-Si	Strain-Si	Si
L [um]	1.5	0.14	0.14	0.08	0.08
EOT [A]	26	?	?	?	14.5
I_d [mA/mm]	85	500	625	930	1650
G_m [mS/mm]	48.5	660	750	1000	1750

I_d/G_m = 50/66 when L = 1.5 μm

I_d/G_m= 87.5/93 when L = 1.5 μm

Considering the differences in L and EOT, our I_d and G_m are comparable to other leading groups.

Comparison between the MBE and ALD films



M. Houssa in Symposium D,
MRS Spring Meeting, April 12-16, 2004.

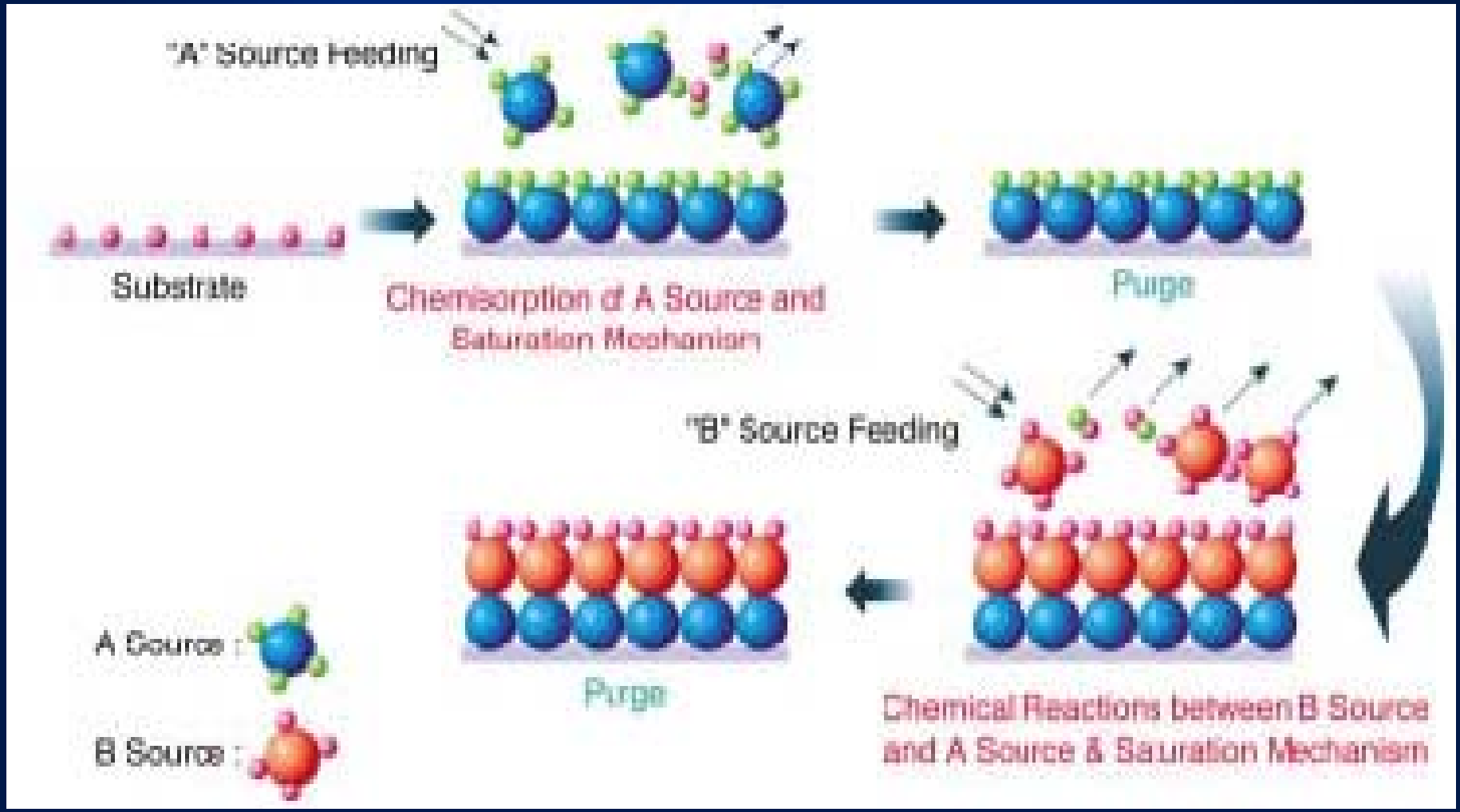
- MBE-grown $Au/HfO_2/Si$ MOS diodes are denoted in red hexagons
- HfO_2 film 4.4 nm thick, with $J_L \sim 10^{-3}$ A/cm^2, κ of 21, an EOT of 0.9 nm
- t_{eq} = EOT

Equivalent Oxide Thickness

$$t_{eq} = t_{ox}\, \kappa_{SiO2} / \kappa_{ox}$$

Atomic Layer Deposition (ALD)

Growth Mechanism : Formation of interfacial SiO_2 is hard to avoid.



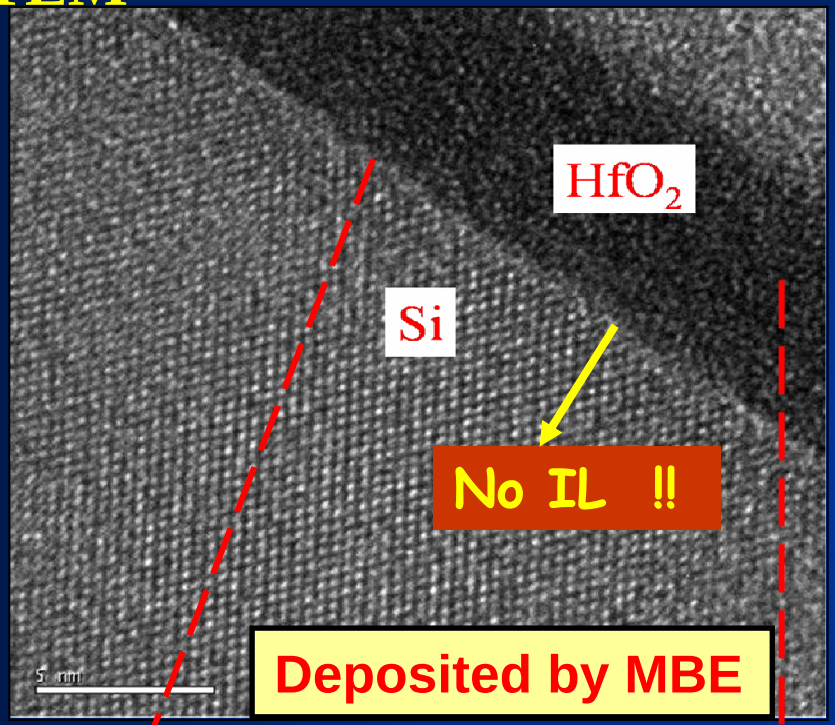
Novel MBE template for ALD growth

Can you make an excellent
HfO_2 Film with a low EOT ?

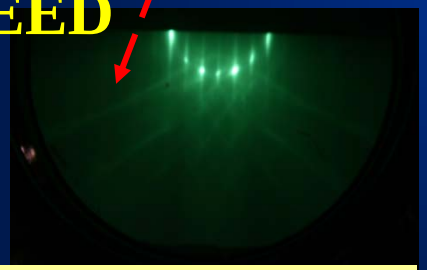
Interface Engineering !

Structural properties of MBE-grown HfO_2

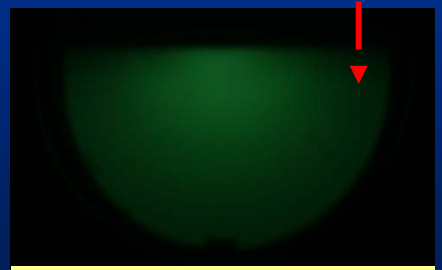
HRTEM



RHEED

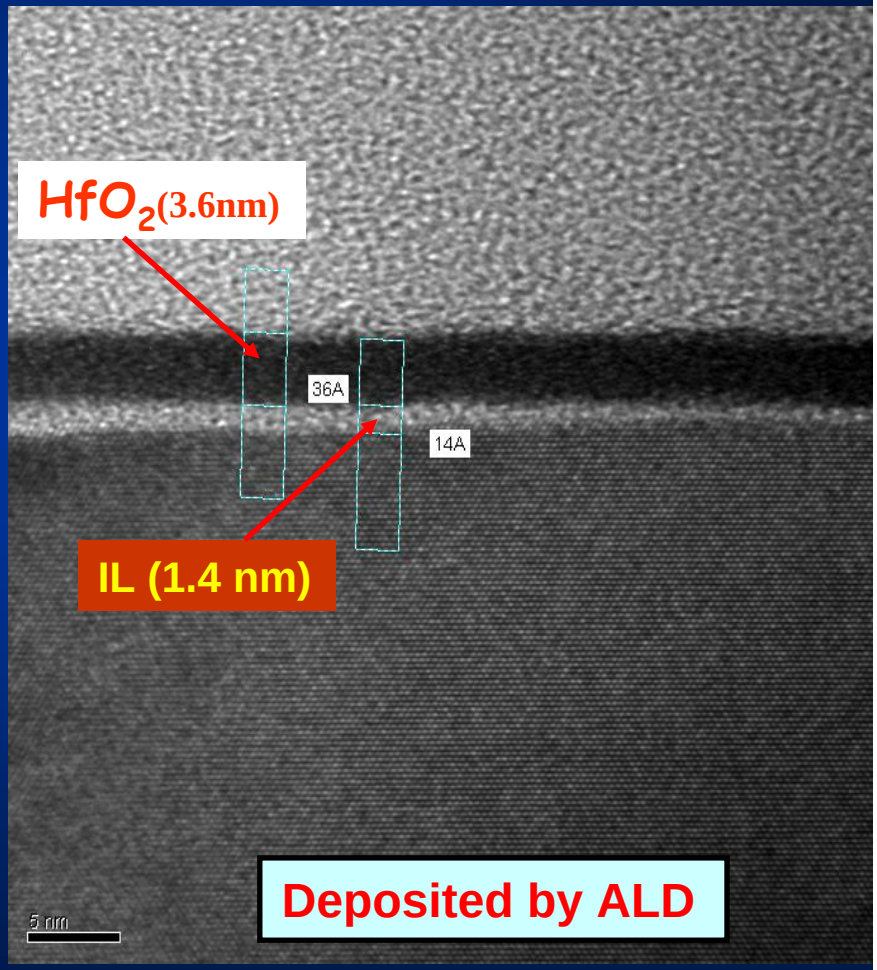


atomically order Si(100) surface



amorphous HfO_2 surface

HRTEM

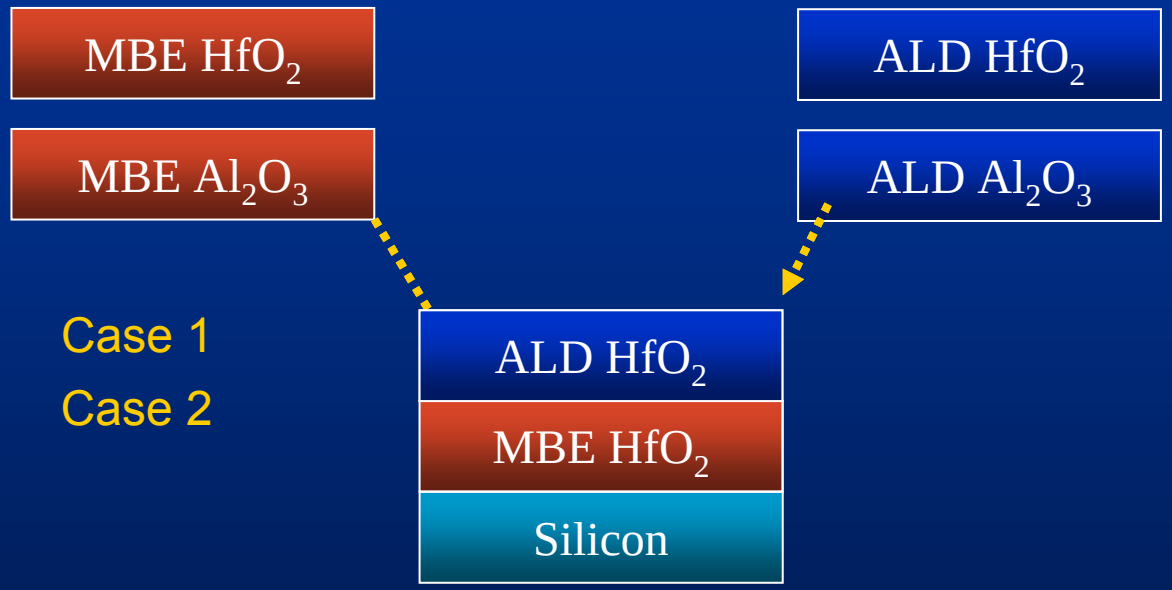


The MBE Template for ALD Growth

MBE and ALD composite film deposition procedure

MBE template film growth

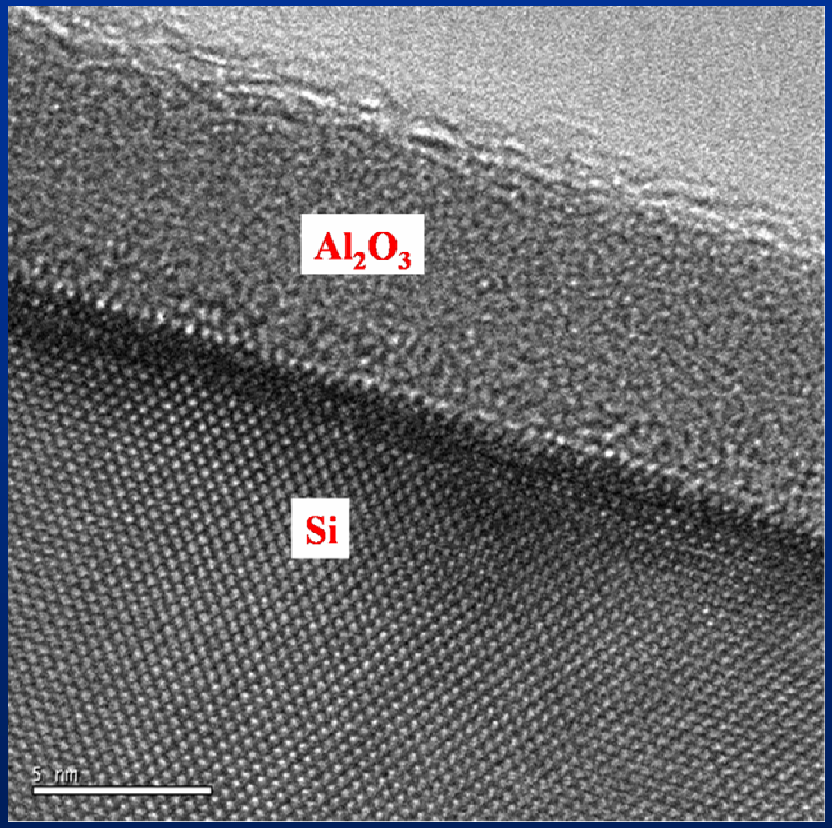
ALD bulk film growth



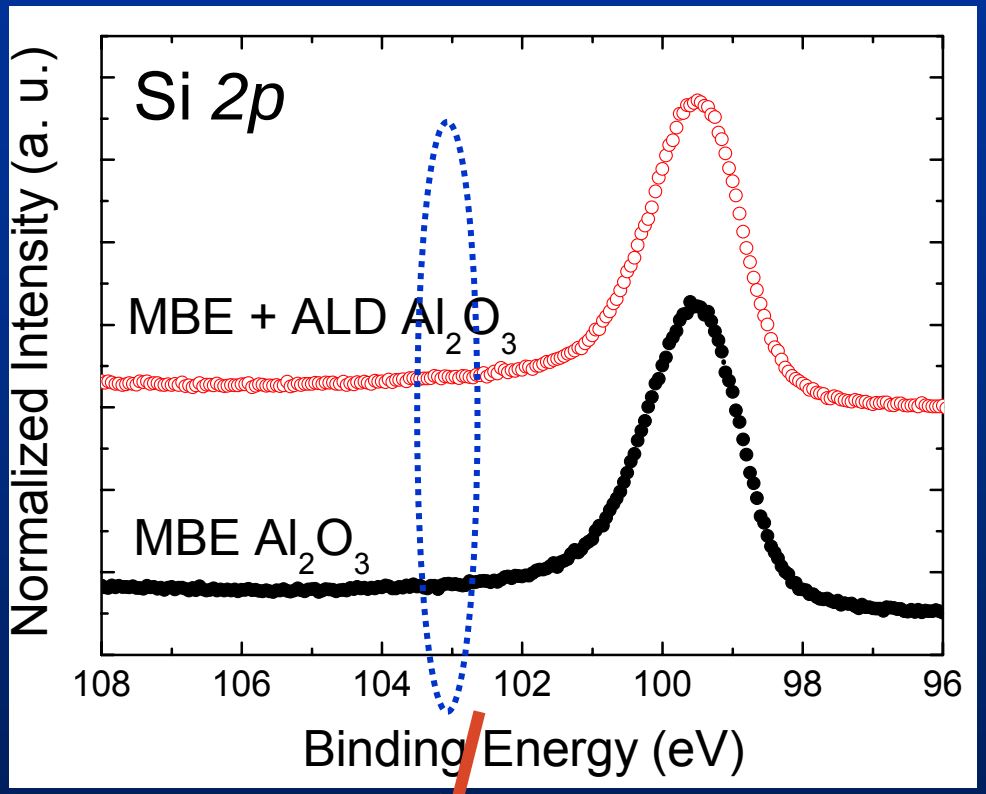
- Low pressure (<1x 10^{-8} torr) maintained during MBE growth
- ALD precursors : TMA, H_2O, $T_{substrate}$: 300℃

The structure of ALD Al_2O_3 with a MBE Al_2O_3 template

TEM



AR-XPS



No peak formed at 103.4eV

→ No SiO_2 formed at interface for both MBE and MBE+ALD Al_2O_3

For HfO_2, have achieved EOT= 0.7 nm

Comparisons of MOSFET Characteristics

	Our work (TiN/..../p-Si)						*Intel*[1]
Dielectrics	**MBE-HfO_2 10nm**	**ALD-HfO_2 10nm**	**YDH 10nm**	**ALD-HfO_2 8nm+ MBE-HfO_2 2nm**	**ALD-HfO_2 4nm+ MBE-HfO_2 2nm**	**YDH 7nm+ Y_2O_3 1nm**	**ALD-HfO_2**
L_g(μm)	1.5	1.5	1.5	**1**	**1**	**1**	**0.08**
EOT(nm)	2.5	3	1.5	**2.5**	**1.5**	**1.6**	**1**
G_m(mS/mm)	35	55	70	**120@V_G=3.5V 100@V_G=2.5V**	**100@V_G=2.5V 1250# 1875***	**125@V_G=2.5V 1560# 2500***	**140 1650**
I_d(mA/mm)	80	55	118	**240@V_G=4V 70@V_G=2.5V**	**155@V_G=2.5V 1940# 2910***	**195@V_G=2.5V 2440# 3900***	**132# 1750**

\# After normaliztion to gate length of 0.08 μm

* After normaliztion to gate length of 0.08 μm and EOT of 1 nm

[1] R. Chau, et al, IEEE Electron Device Letters **25**, No. 6, 408 (2004)

Major Research Accomplishment

- First demonstration of atomically abrupt high k HfO_2/Si interface.

- Successful integration of the 6 inch Si CMOSFET processing in NDL with our 2” MBE high κ dielectric films using a TiN metal gate to produce a gate length 1.5 mm transistor device.

- Novel ALD + MBE template approach, superior electrical performance.