Advances in High κ Dielectrics For Si and GaAs Nano Electronics

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近年奈米科技之發展

- 縮小尺度至100 nm以內的科技：
  Top-down之奈米結構的雕刻細化
  莫爾定律(Moore’s law－每1.5年縮小30%尺寸)

- 操控原子（分子）的科技：Bottom-up 之奈米體系的成長組裝
  費曼的主張－從底部作起，下面還有無限寬廣的空間

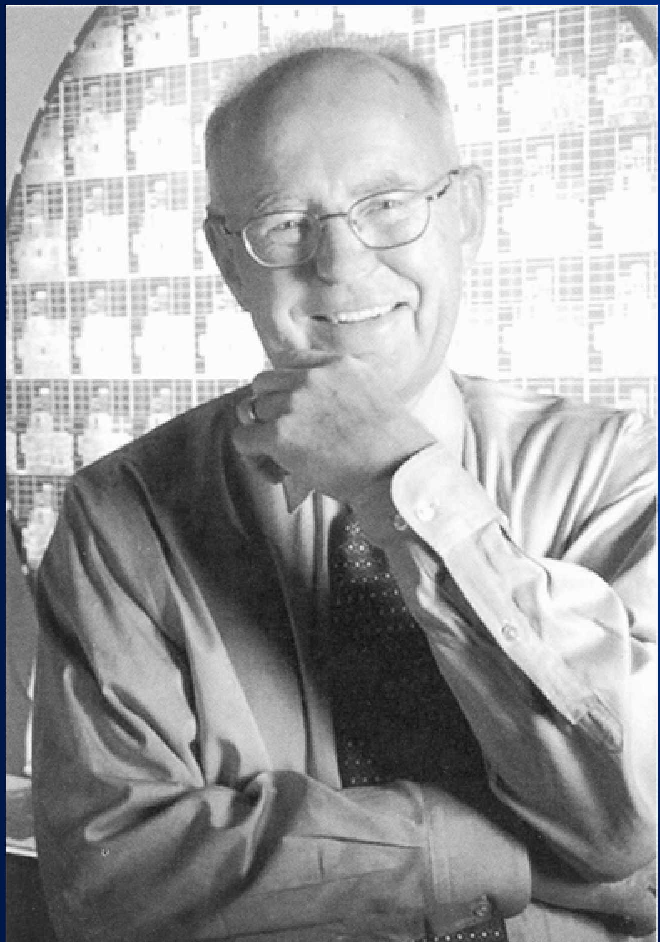
近來大力推動奈米科技的背景

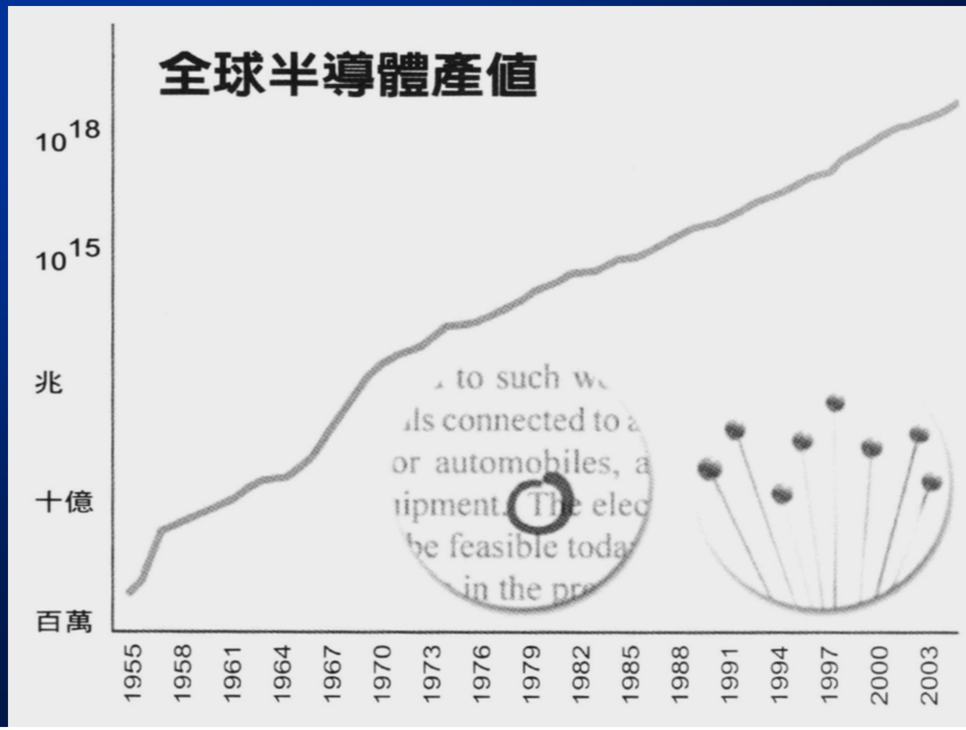
來自微電子學可能遭遇瓶頸的考慮

Moore‘s Law：摩爾定律

A 30% decrease in the size of printed dimensions every 1.5 years.

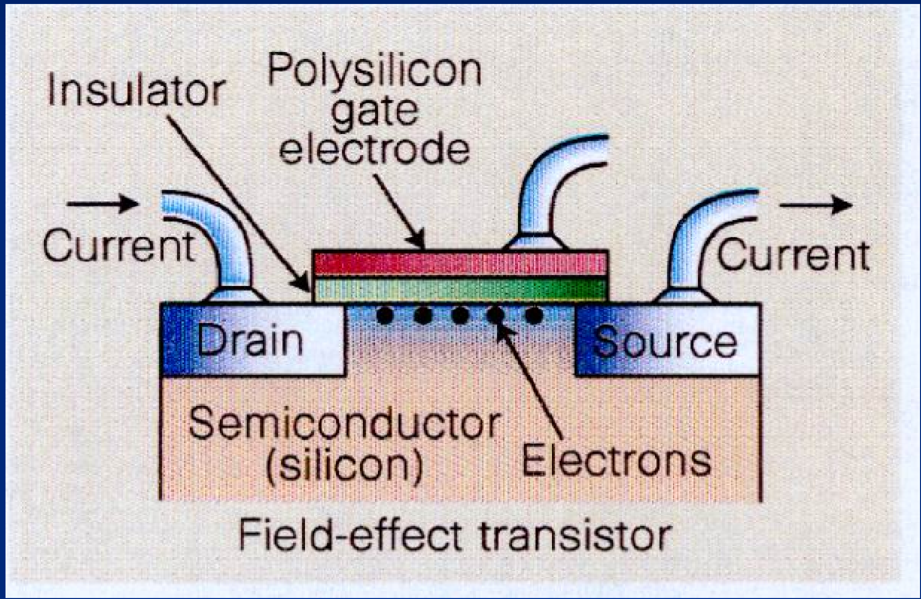
矽晶上電子原件數每1年半會增加一倍





Device Scaling, Moore's Law

1960 Kahng and Atalla,   First MOSFET



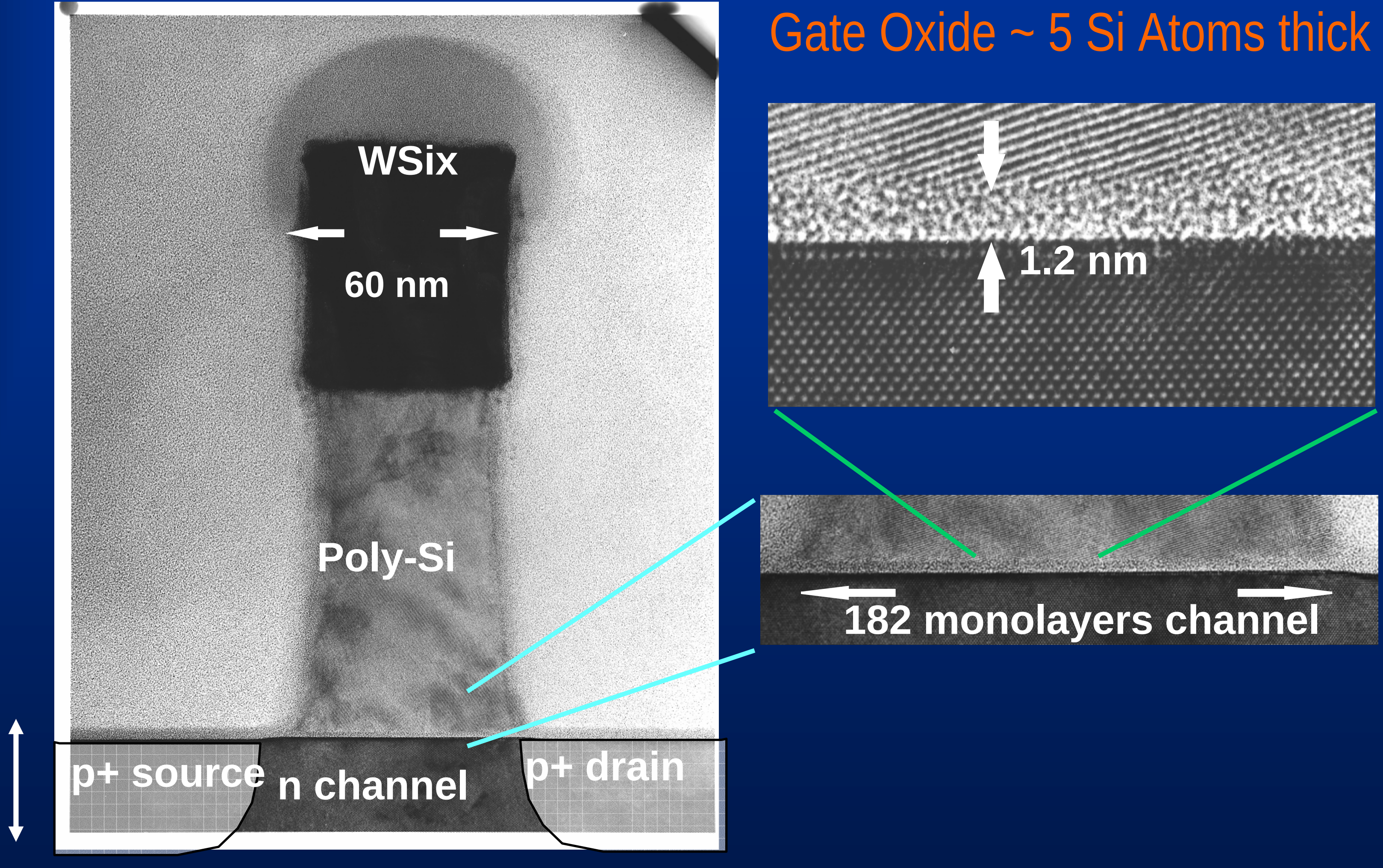
Moore's Law:
The number of transistors per square inch doubles every 18 months

Shorter gate length L
Thinner gate dielectrics t_{ox}

Driving force :
High speed
Lower power consumption
High package density

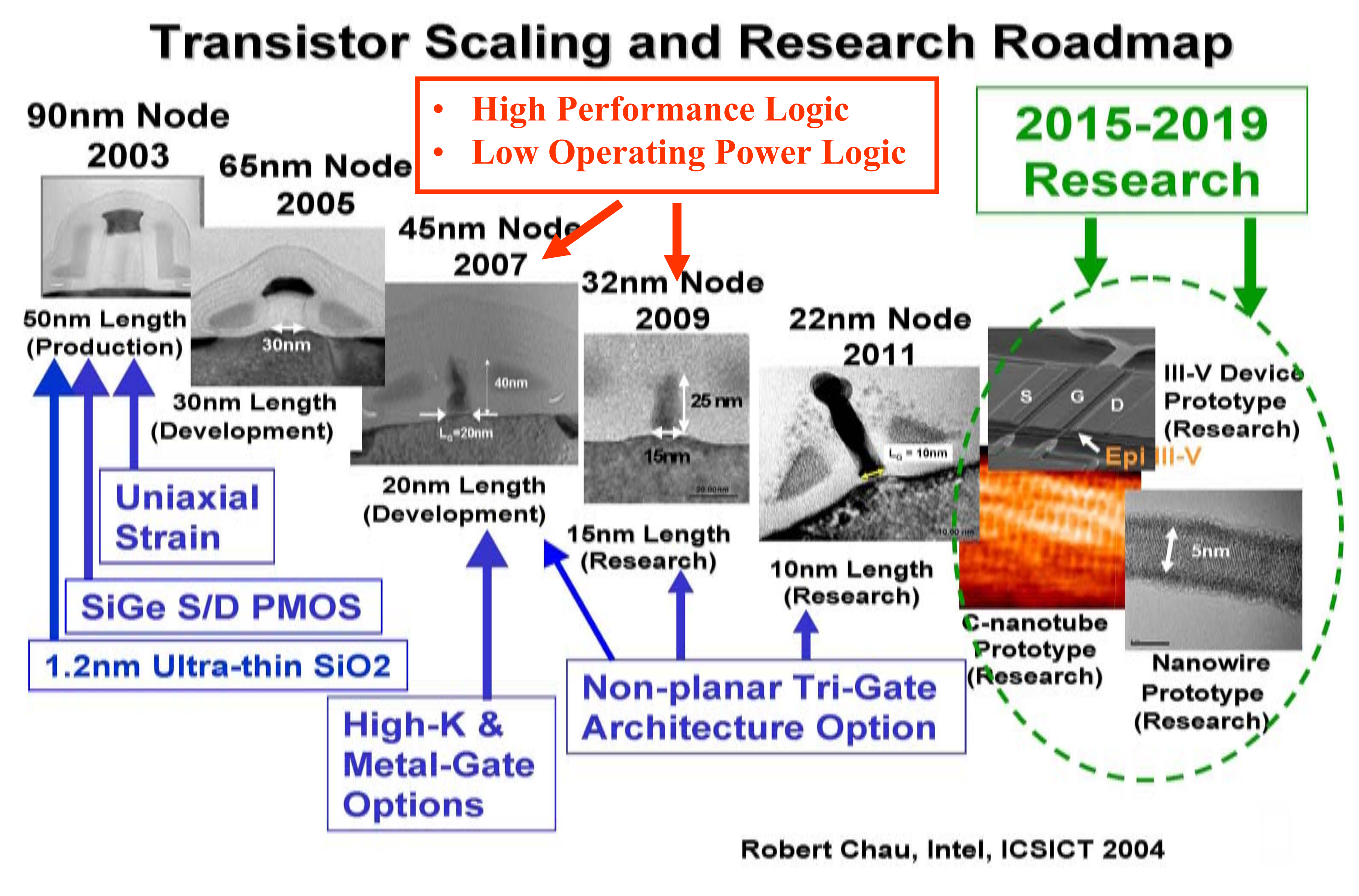
Scaling Limits to CMOS Technology

Gate Oxide ~ 5 Si Atoms thick !



Shrinking the junction depth ➡ increasing the carrier concentration

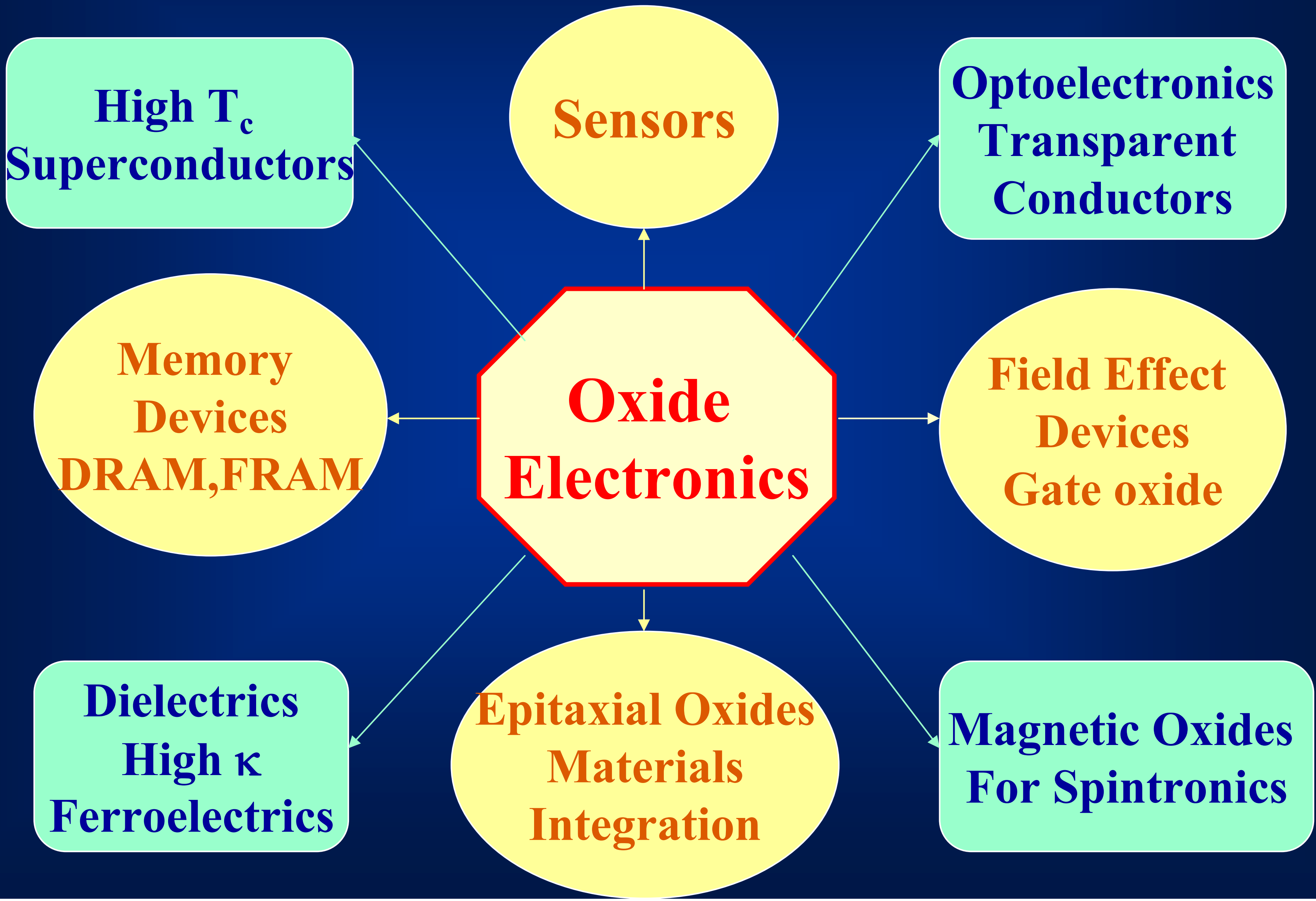
Intel Transistor Scaling and Research Roadmap



TALK OUTLINES

- The alternative high κ gate dielectrics replacing SiO_2 for 33 nm Si CMOS by year 2009
  - -- Materials requirements
  - -- Processing integration issues
- MBE grown HfO_2 high κ gate dielectrics
  - -- thermal stability studies by MEIS and TEM
  - -- electrical performance
- Integration of high κ dielectrics with metal gate
  - -- $TiN/HfO_2/Si$ high κ MOSCAPs and MOSFETs
- New high κ dielectrics such as HfO_2 for GaAs based electronics

The Development of Oxide Electronics in Two Decades



CMOS scaling, When do we stop ?

Reliability: 25 ~~22~~ ~~18~~ ~~16~~ Å

processing and yield issue

Tunneling : 15 Å

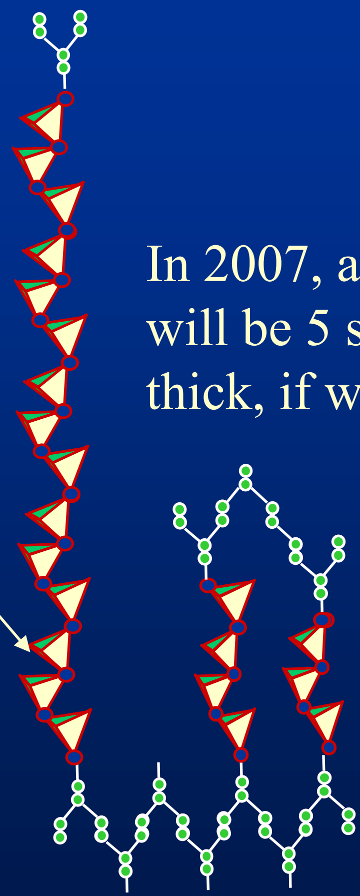
Design Issue: chosen for $1 A/cm^2$ leakage
$I_{on}/I_{off} >> 1$ at 12 Å

Bonding:

Fundamental Issues---

- how many atoms do we need to get bulk-like properties?
  EELS -- Minimal 4 atomic layers !!
- Is the interface electronically abrupt?
- Can we control roughness?

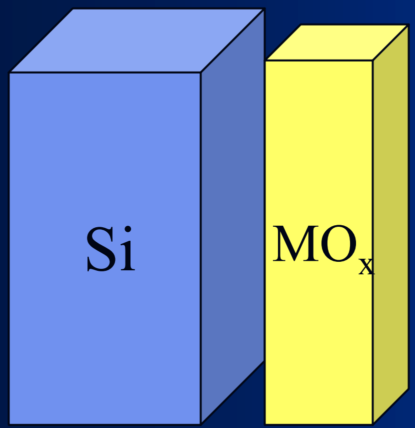
In 1997, a gate oxide was 25 silicon atoms thick.



In 2007, a gate oxide will be 5 silicon atoms thick, if we still use SiO_2

and at least 2 of those 5 atoms will be at the interfaces.

Fundamental Materials Selection Guidelines



$Si + MO_x \longrightarrow M + SiO_2$

$Si + MO_x \longrightarrow MSi_2 + SiO_2$

$Si + MO_x \longrightarrow MSiO_x + SiO_2$

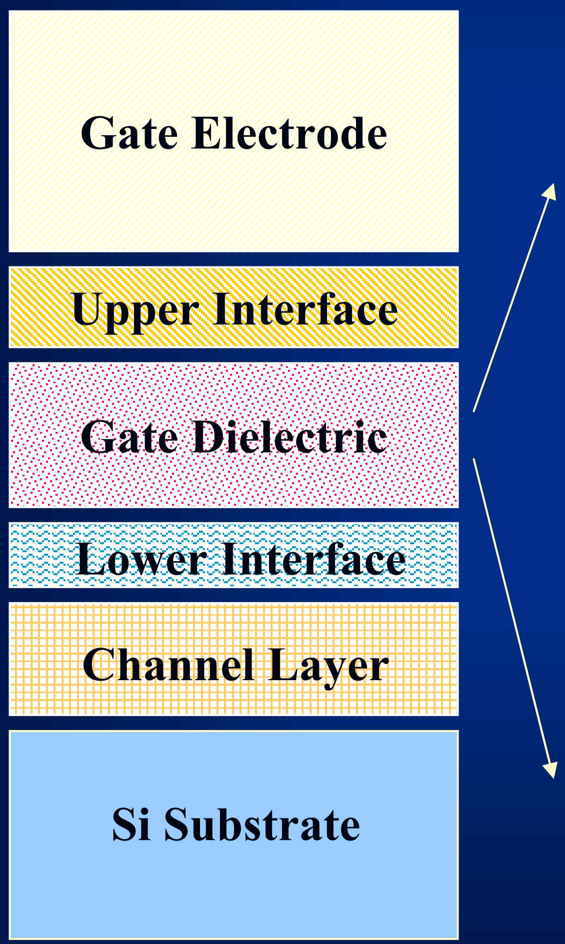
- Thermodynamic stability in contact with Si to 750ºC and higher. **(Hubbard and Schlom)** **Alkaline earth oxide, IIIB, IVB oxide and rare earth oxide**
- Dielectric constant, band gap, and conduction band offset
- Defect related leakage, substantially less than SiO_2 at $t_{eq} < 1.5$ nm
- Low interfacial state density $D_{it} < 10^{11}\ eV^{-1}cm^{-2}$
- Low oxygen diffusivity
- Crystallization temperature >1000°C

t_{eq} : **equivalent oxide thickness (EOT) to be under 1.0 nm**

$t_{eq} = t_{ox}\ \varepsilon_{SiO2} / \varepsilon_{ox}$

Integration Issues for High κ Gate Stack

FET Gate Stack



Critical Integration Issues

- Morphology dependence of leakage
  Amorphous vs crystalline films?
- Interfacial structures
- Thermal stability
- Gate electrode compatibility
- Reliability

Fundamental Limitations

- Fixed charge
- Dopant depletion in poly-Si gate
- Dopant diffusion
- Increasing field in the channel region

Basic Characteristics of Binary Oxide Dielectrics

Dielectrics	SiO_2	Al_2O_3	Y_2O_3	HfO_2	Ta_2O_5	ZrO_2	La_2O_3	TiO_2
Dielectric constant	3.9	9.0	18	20	25	27	30	80
Band gap (eV) Band offset (eV)	9.0 3.2	8.8 2.5	5.5 2.3	5.7 1.5	4.5 1.0	7.8 1.4	4.3 2.3	3.0 1.2
Free energy of formation $MO_x+Si_2 \longrightarrow M+ SiO_2$ @727C, Kcal/mole of MO_x	-	63.4	116.8	47.6	-52.5	42.3	98.5	7.5
Stability of amorphous phase	High	High	High	Low	Low	Low	High	High
Silicide formation ?	-	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Hydroxide formation ?	-	Some	Yes	Some	Some	Some	Yes	Some
Oxygen diffusivity @950C (cm^2/sec)	$2x\ 10^{-14}$	$5x\ 10^{-25}$	?	?	?	10^{-12}	?	10^{-13}

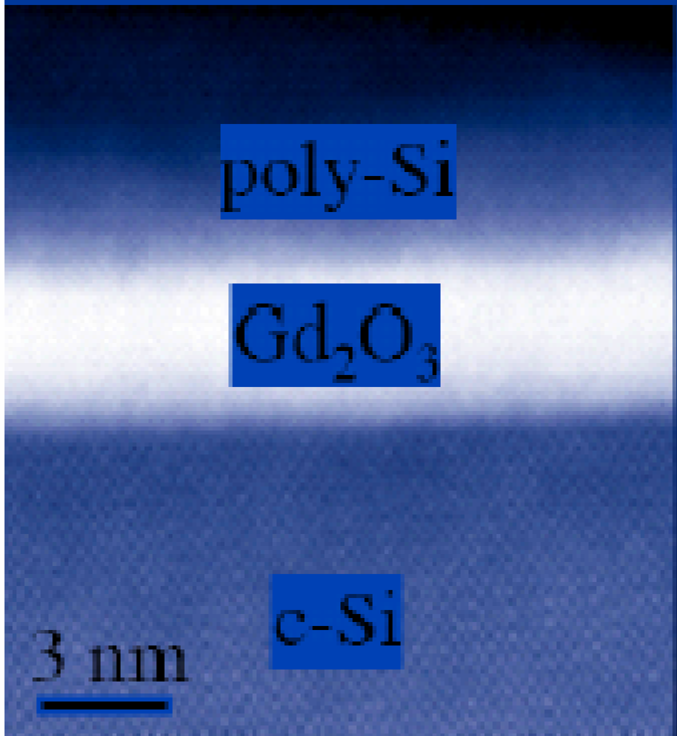
Assessing Thermodynamic Stability

Gate Dielectric Material

Silicon

Ideal "Gedanken" Interface

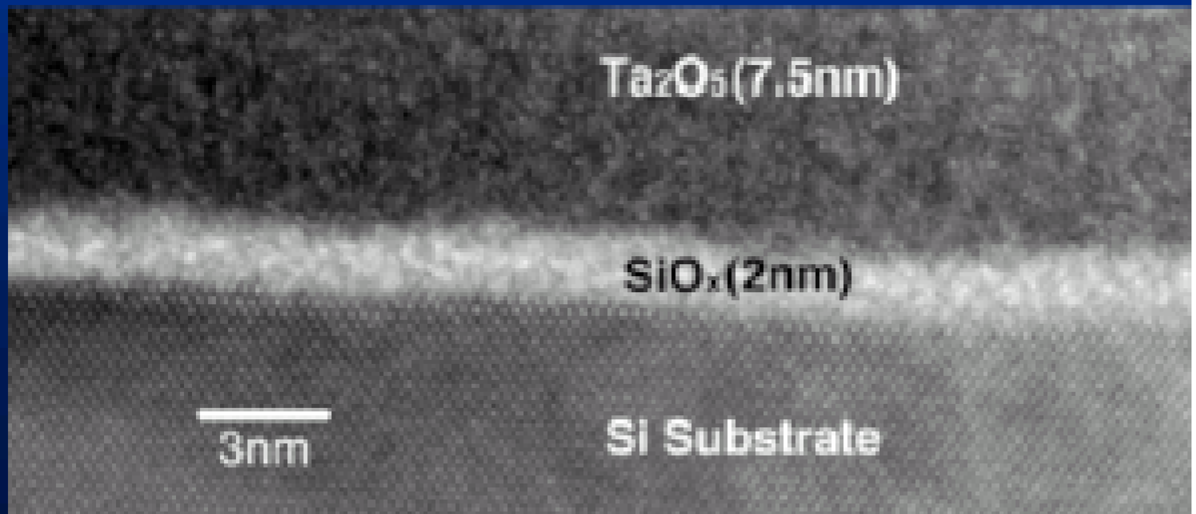
Stable Interface



TEM by David A. Muller

J. Kwo *et al.*, J. Appl. Phys. 89 (2001) 3920.

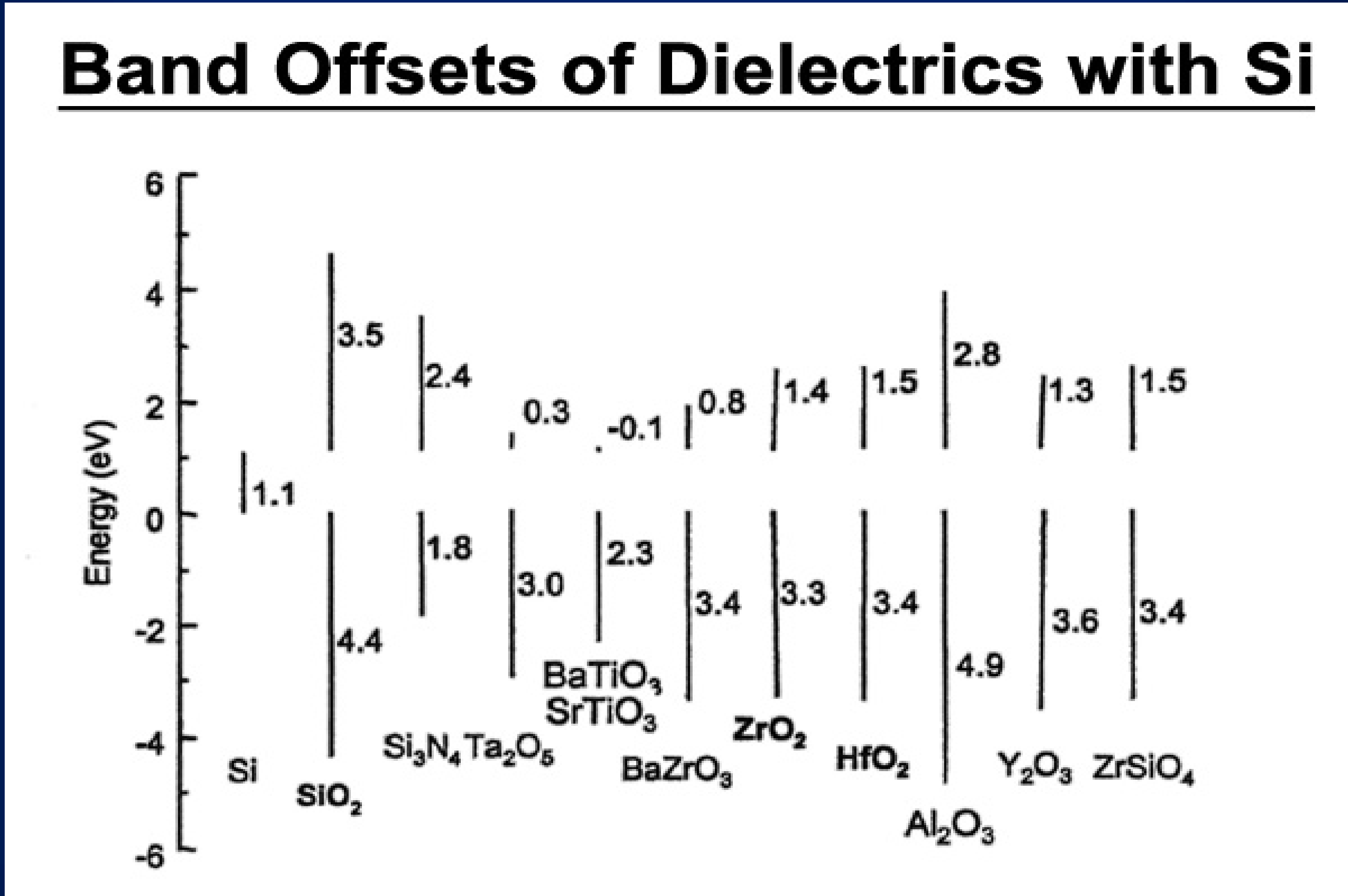
Unstable Interface



TEM by Don J. Werder

G.B. Alers *et al.*, Appl. Phys. Lett. 73 (1998) 1517.

Band Offset of High κ Dielectrics



J. Roberson, JVST 18, 1785, (2000)

A Topic Well Worth Doing Research On !!!

World production in year 2003: 1 x 10^{18} transistors

World population: 6.4 x 10^{9} people

So, the world produces:

- ~ 1.5 x 10^{8} transistors/person each year
- ~ 1.2 x 10^{7} transistors/person each month
- ~ 400,000 transistors/person each day
- ~ 300 transistors/person each minute
- ~ 5 transistors/person per second

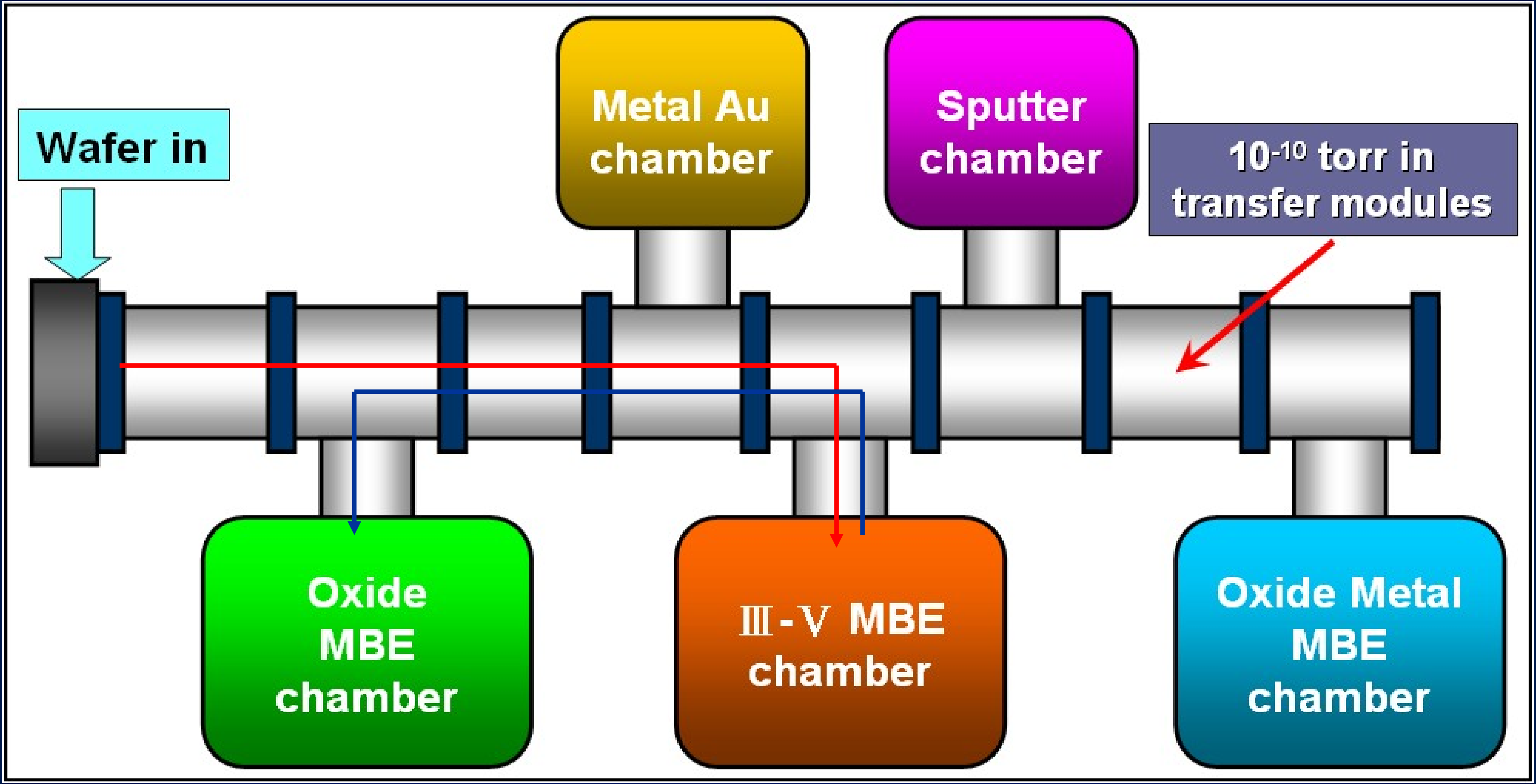
And Taiwan produces ~ 500 transistors/person/per second

MBE Integrated Multi-chamber System For Nano Electronics

Now located in the Nano Technology Center, ITRI, Hsin Chu, Taiwan since 7/2003.

In-situ Fabrication

UHV integrated processing system



Multichamber Ultrahigh Vacuum System

1. A solid source GaAs-based MBE chamber
2. Oxide deposition chamber (As-free)
3. UHV transfer modules

Research Programs

- Low defect high κ ultrathin films
  --Interface engineering
  --Electrical characterization and optimization

- Identify new material candidates for metal gate
  --Metal gate/high κ integration

- Integration of high κ, and metal gate with Si- Ge strained layer
  Integration of high κ, and metal gate with strained Si

- High k dielectrics for high mobility III-V semiconductors

High κ Dielectrics for Si

- Epitaxial crystalline films on Si

  (A) Cubic CaF_2 structure:

  (111) orientation is more common than (100)

  e.g. Ca F_2 (111), CeO_2 (111) on Si(111) with ε ~ 26

  YSZ (100) on Si(100) with ε~ 25-30

  (B) Cubic Mn_2O_3 structure

  ~ 8 unit cells of incomplete fluorite structure

  e.g. Y_2O_3 (110) on Si(100) with ε ~ 16-18

  Gd_2O_3 (110) on Si(100) with ε ~ 12-14

  (C) Ternary perovskite structure

  e.g. $SrTiO_3$ (100) on Si(100) with ε~ 70-80 (Oakridge, Motorola)

  using a Sr silcide ¼ monolayer for epi-growth

- Amorphous oxide films on Si

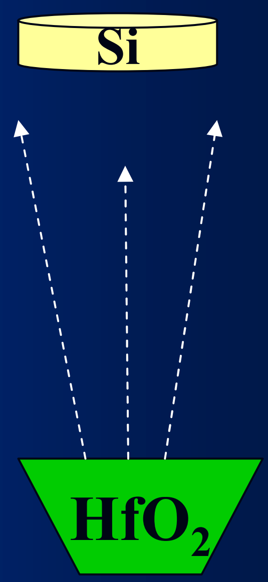
  e.g. Si_3N_4 , Al_2O_3 , Ta_2O_5 , ZrTiSnOx, TiO_2 Interfacial layer present

  - Amorphous Gd_2O_3 and Y_2O_3 films,

  - Amorphous SiO_2 added with Hf or Zr . (G. Wilks et al)

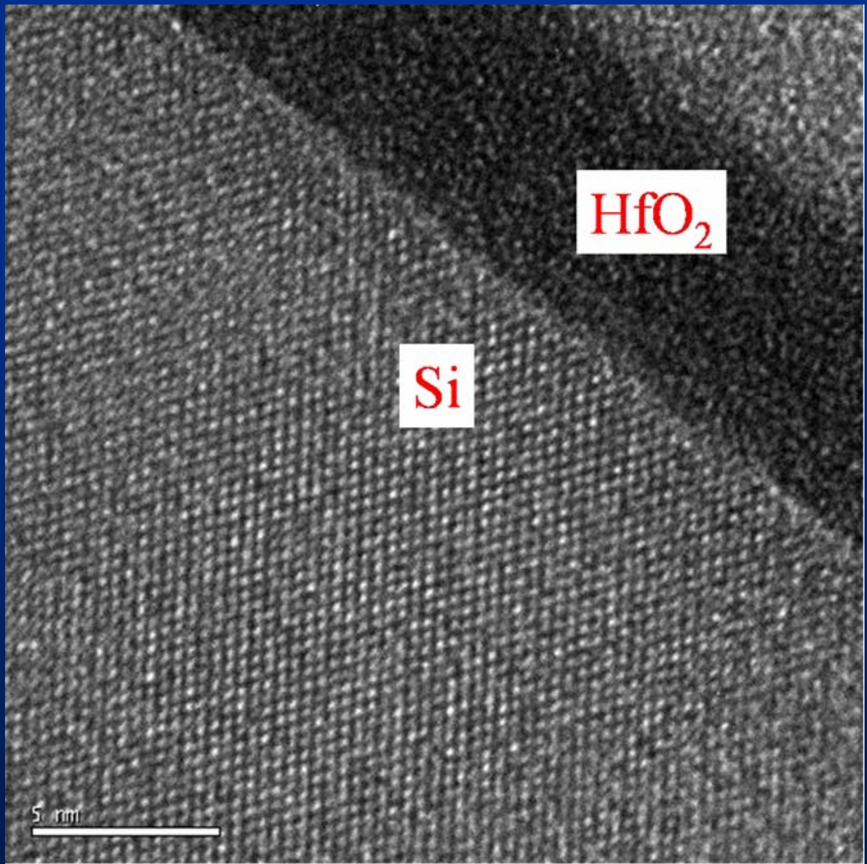
MBE Growth of High κ Oxides

- Ultrahigh vacuum, multi-chamber MBE system.
- Electron-beam evaporation of oxide sources from pressed ceramic pellets.
- 2 inch RCA-cleaned Si wafers, hydrogen passivated, followed by prompt insertion into UHV.
- In-situ heating to 400-500C to attain a (2 x 1) reconstructed Si surface.
- Substrate temperature of 550C for **epitaxial** films.
- Room temperature deposition for **amorphous** films.
- Maintain **low pressure** during growth $< 1.0 \times 10^{-9}$ torr.



High Resolution Cross Sectional TEM and RHEED Images of HfO_2 on Si (100)

From AFM: RMS Roughness: 0.072nm



Amorphous HfO_2 film 6.0 nm

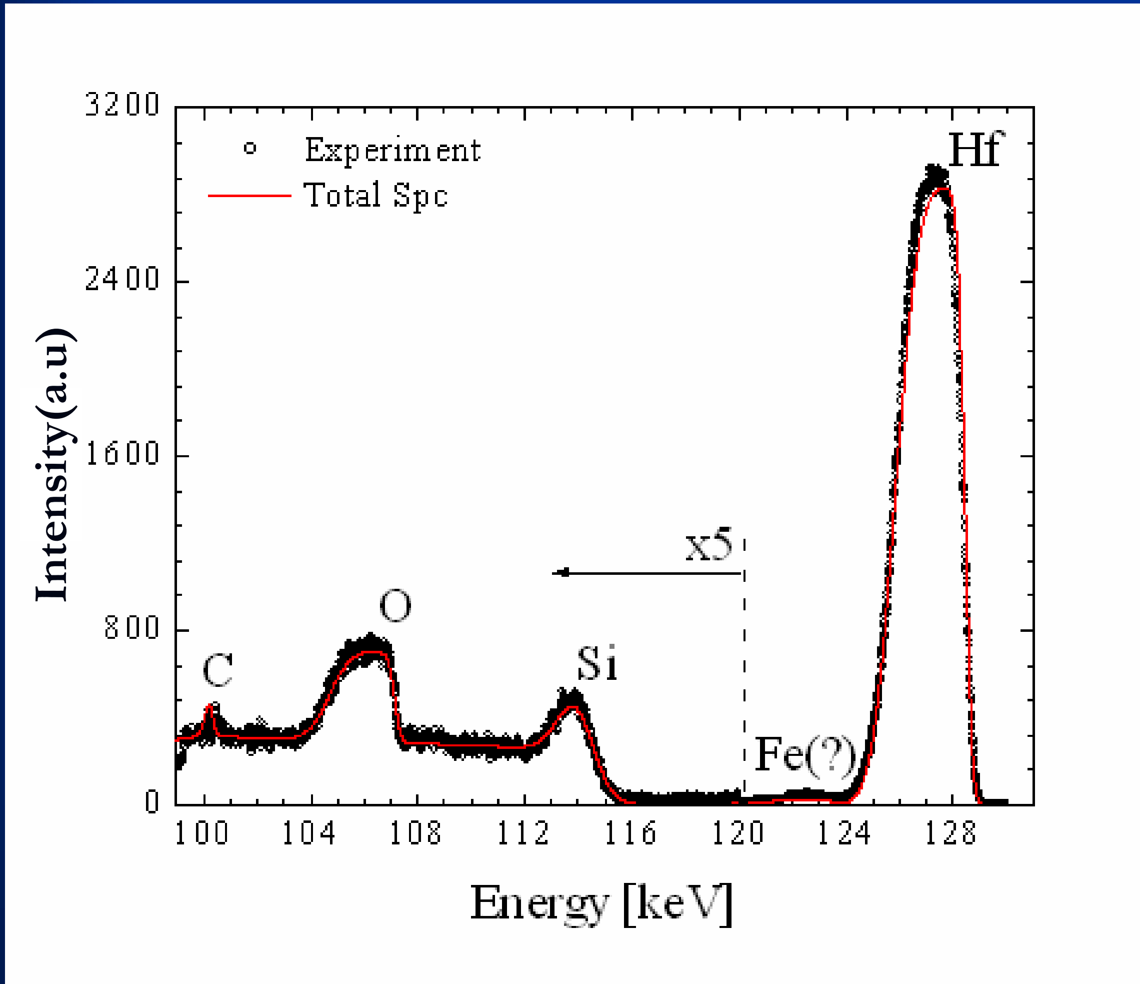
SiO_2 and Hf silica is nearly absent !

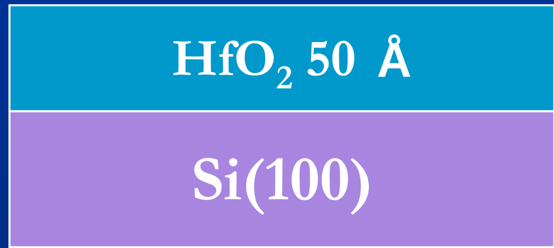
RHEED

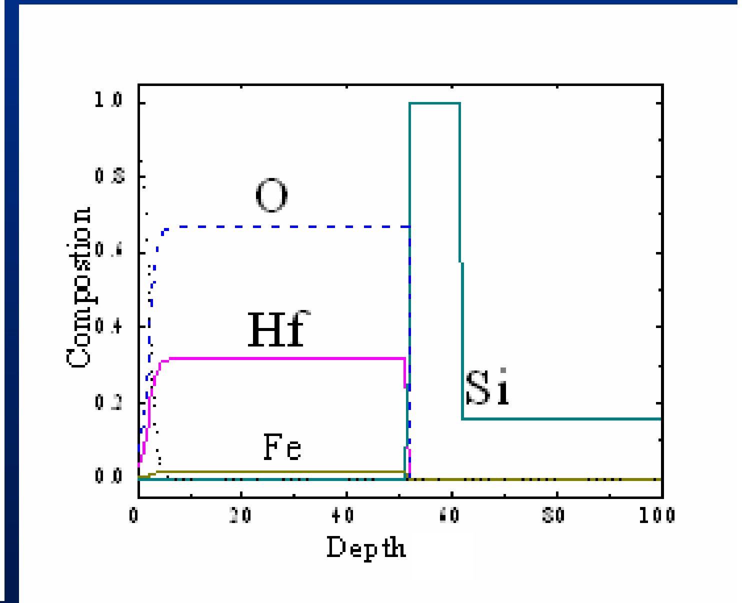
amorphous HfO_2 surface

atomically order Si(100) surface

Medium Energy Ion Scattering (MEIS) Study of the High κ Dielectric / Si Interface and Stability

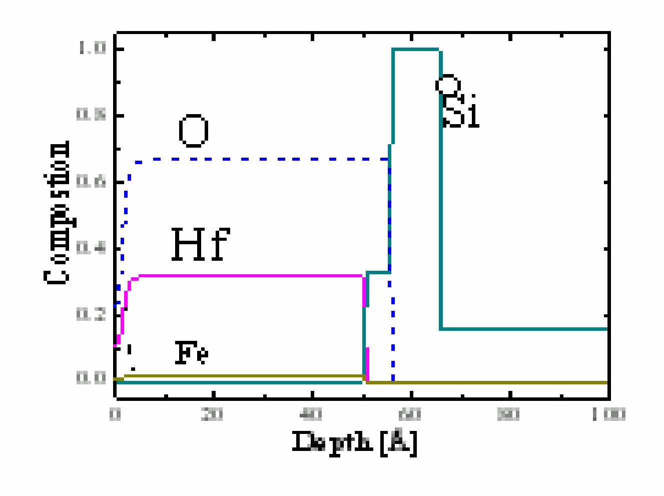




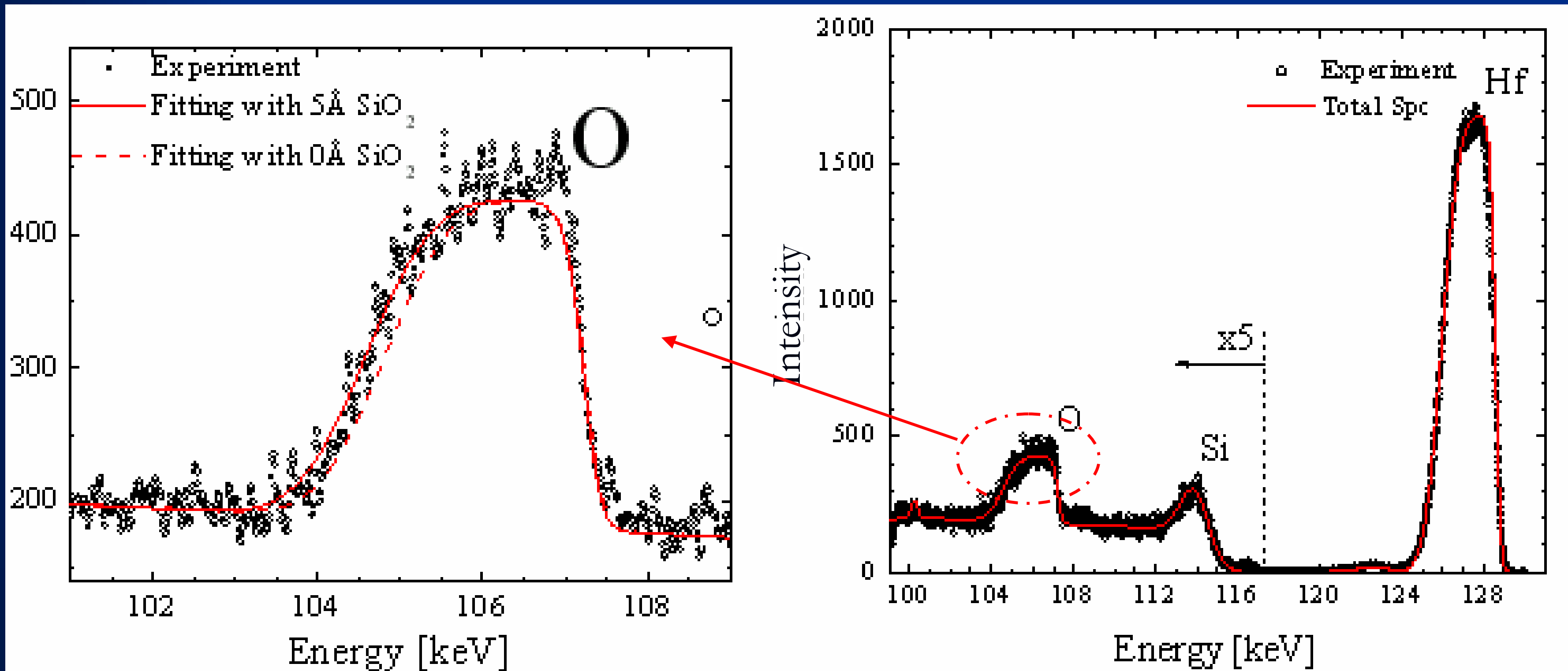


With Rutgers University using 130 keV proton beam
It shows the absence of silica near the interface.

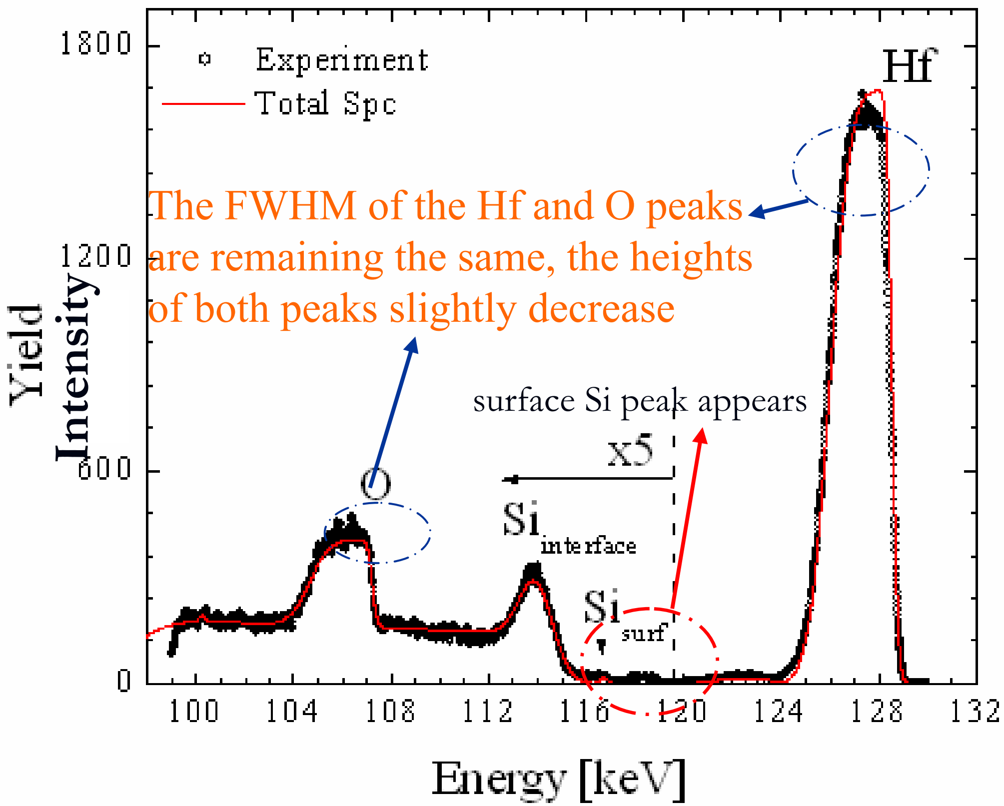
Vacuum annealing at 630°C



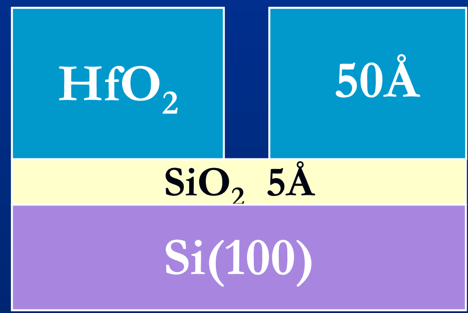
Broadening of the O peak and small increase in the Si peak indicate some interfacial SiO_2 formation about 0.4 nm.



Annealing from 630°C to 950°C

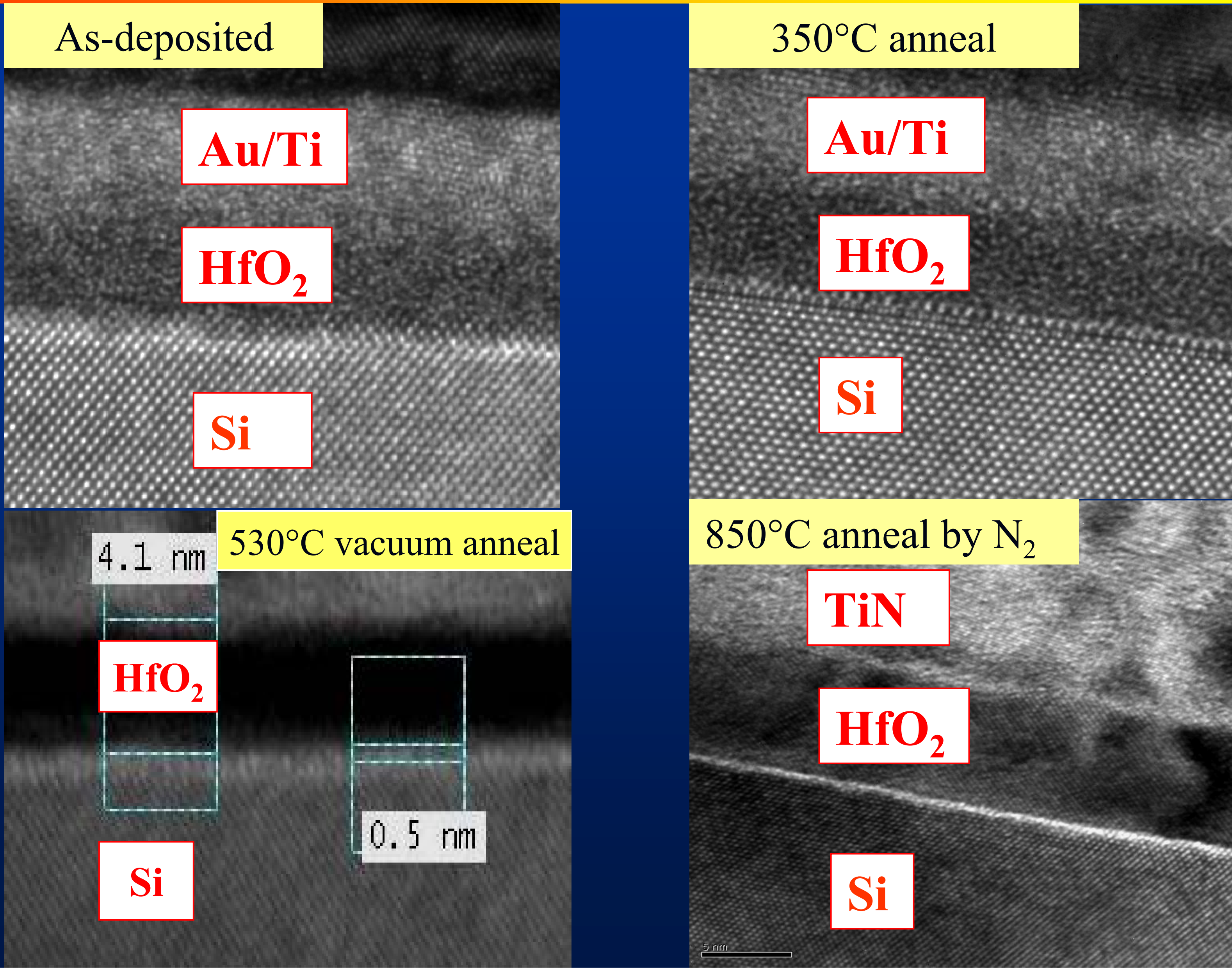


A possible structure after high temperature anneal

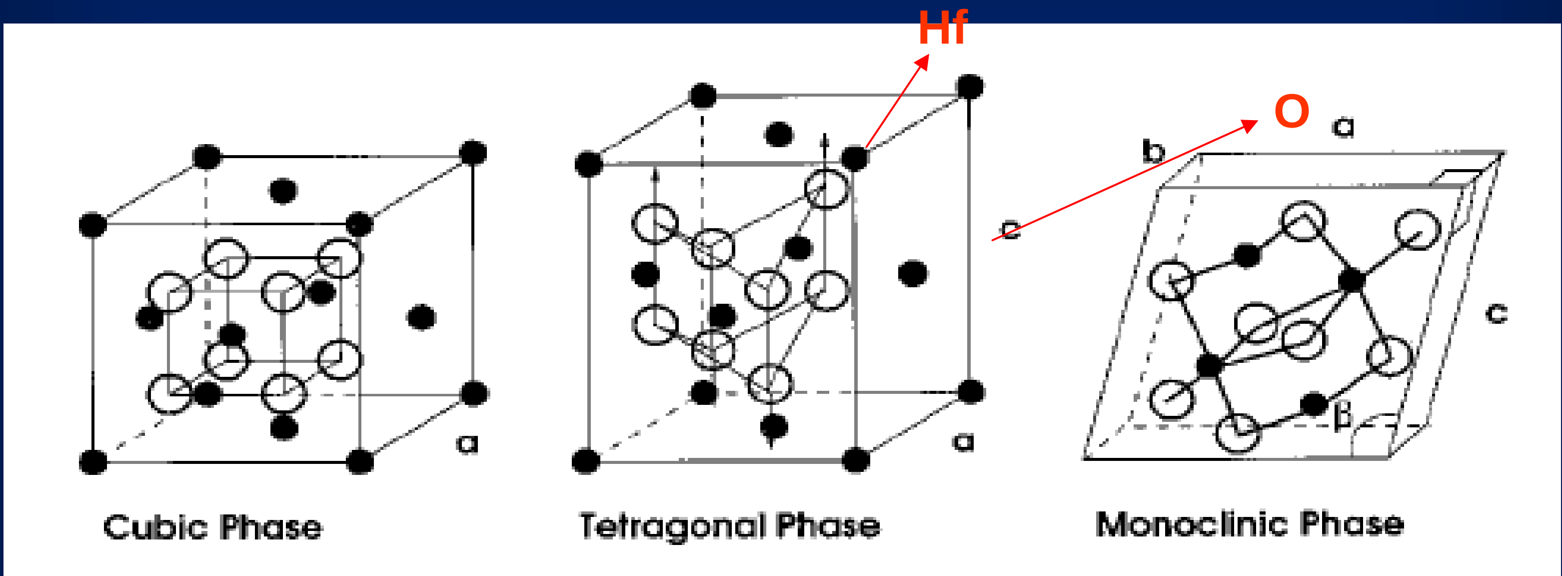


Discontinuities and islands were formed in HfO_2 .

HRTEM Study of Thermal Stability of High κ HfO_2 Gate Stacks



Change the structure of HfO_2



Dielectric constants

29 70 16

If we could change the structure of HfO_2 from monoclinic to other structure, we would increase the dielectric constant .

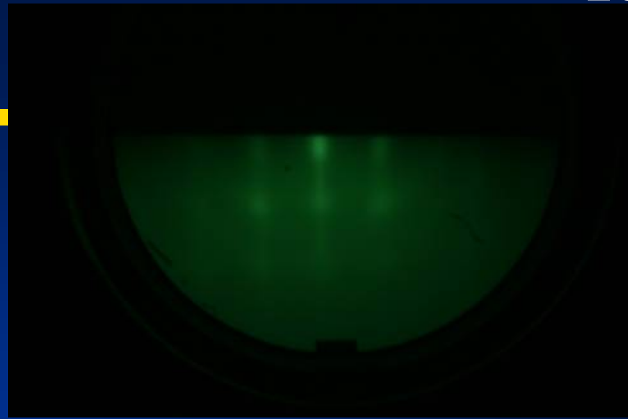
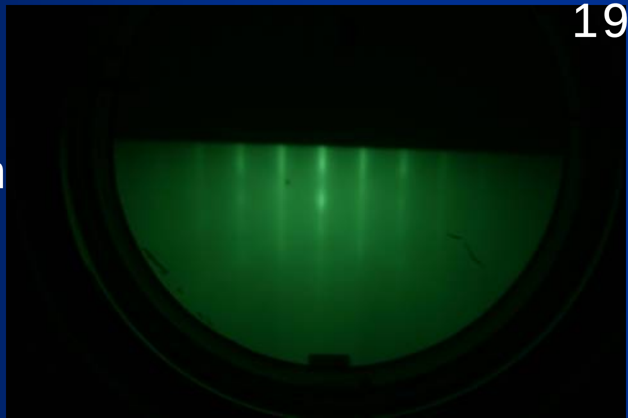
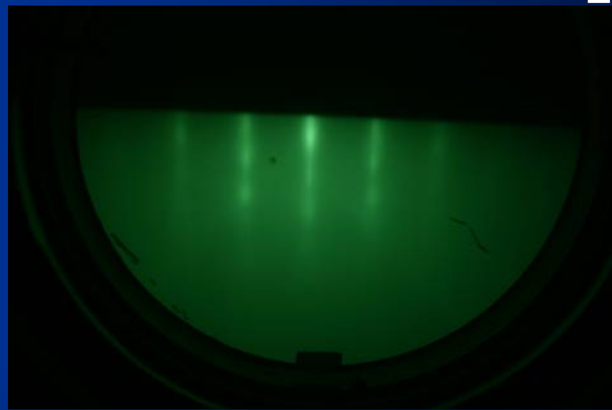
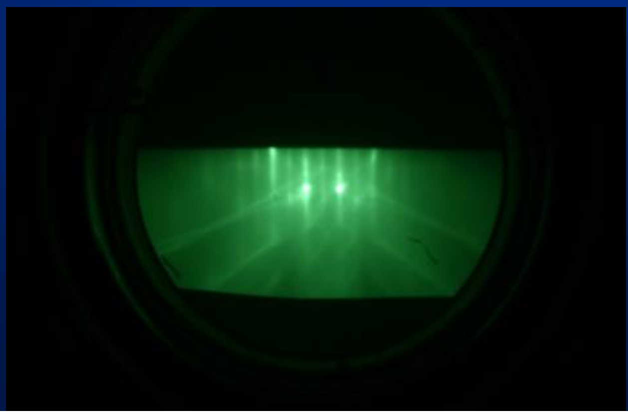
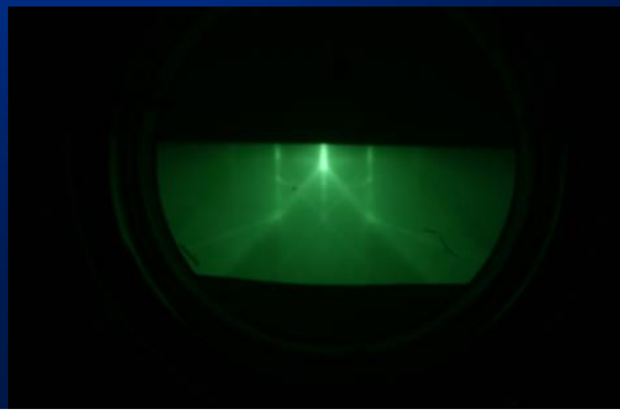
Xinyuan Zhao and David Vanderbrit PHYSICAL REVIEW B, VOLUME 65, 233106

Permittivity Increase of Yttrium-doped HfO_2 Through Structural Phase Transformation

by Koji Kita, Kentaro Kyuno, and Akira Toriumi, Tokyo Univ.

HfO_2	<1750℃	**monoclinic**	**κ~16-18**
	>1750℃	**cubic**	**κ~29**
	>2700℃	**tetragonal**	**κ~70**

- Yttrium serves effectively as a dopant to induce a phase transformation from the ***monoclinic*** to the ***cubic*** phase even at 600 °C.
- Yttrium-doped HfO_2 films show higher permittivity than undoped HfO_2, and the permittivity as high as 27 is obtained by 4 at. % yttrium doping.
- The permittivity of undoped HfO_2 is reduced significantly at high temperature, whereas that of 17 at. % yttrium-doped film shows no change even at 1000 °C.

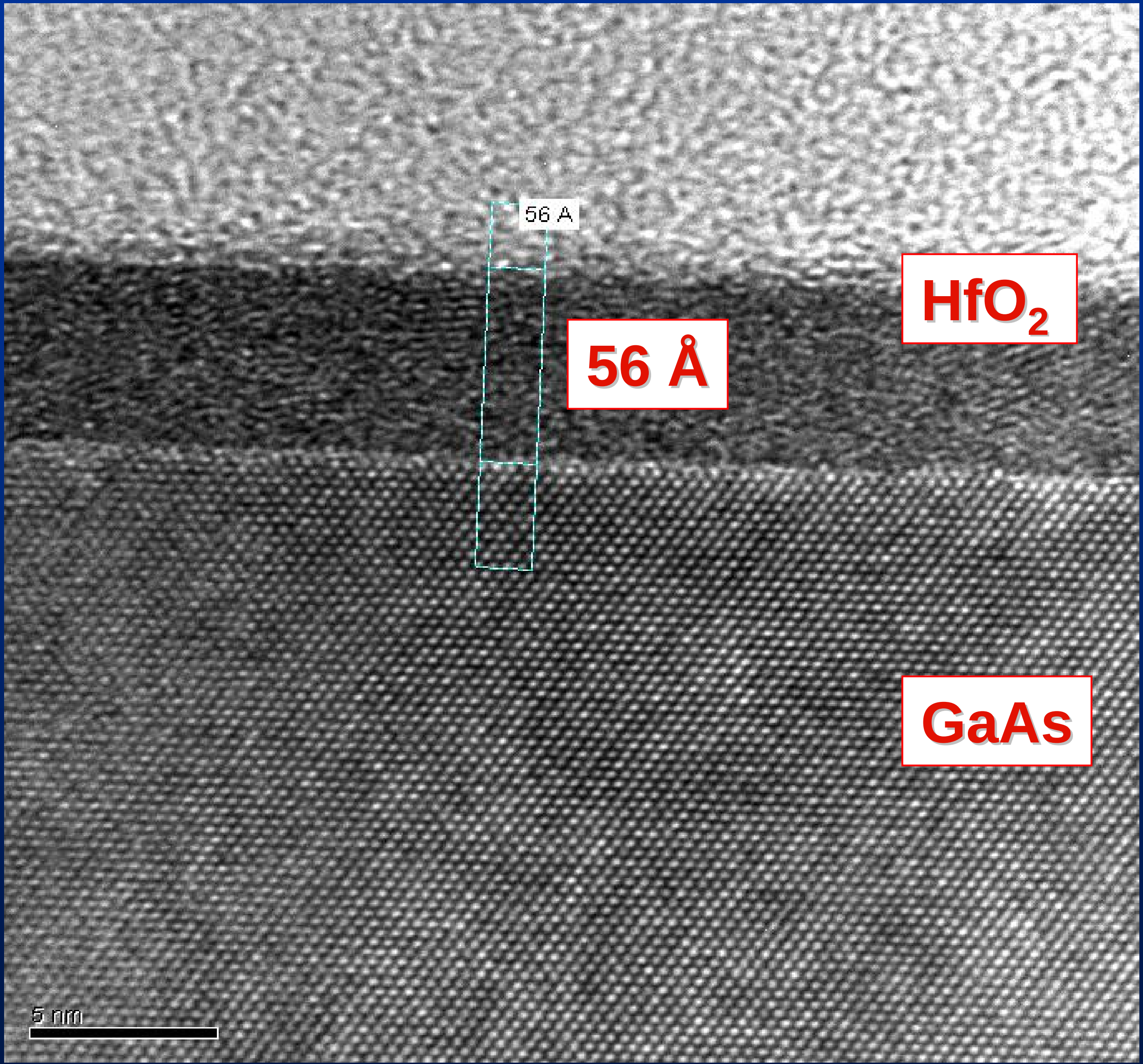
	2x position	1x position
After deposition for 5mins Dielectric film of 4 –fold symmetry in the plane	190 ° 	280 ° 
After deposition for 2mins	190 ° 	280 ° 
After reconstruction	145 ° 	235 ° 

Wafer rotate22.5 °

HRTEM of Low Temp Growth

amorphous HfO_2 on GaAs (100)

A very abrupt transition from GaAs to HfO_2 over one atomic layer thickness was observed.

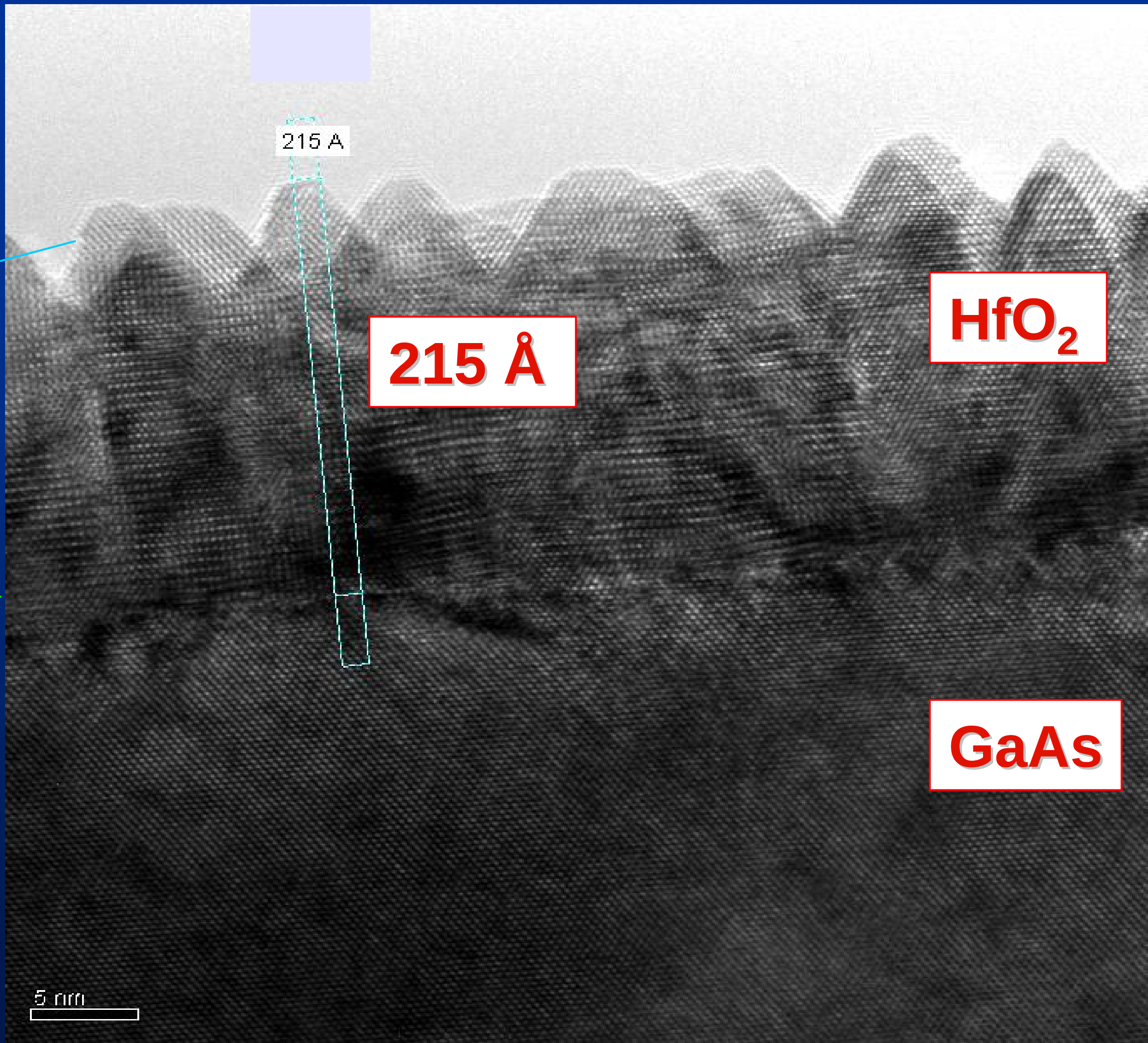


HRTEM of High Temp Growth

Epitaxial HfO_2 film grown on GaAs (100) at 620℃

The air/HfO_2 surface is very rough.

The interface between HfO_2 and GaAs is not sharp.

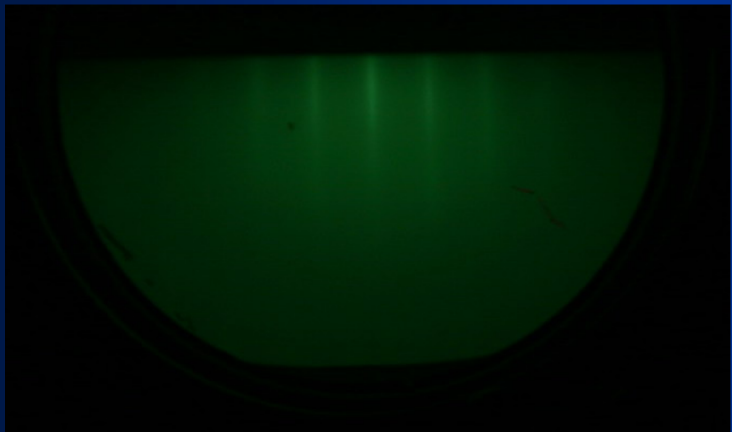


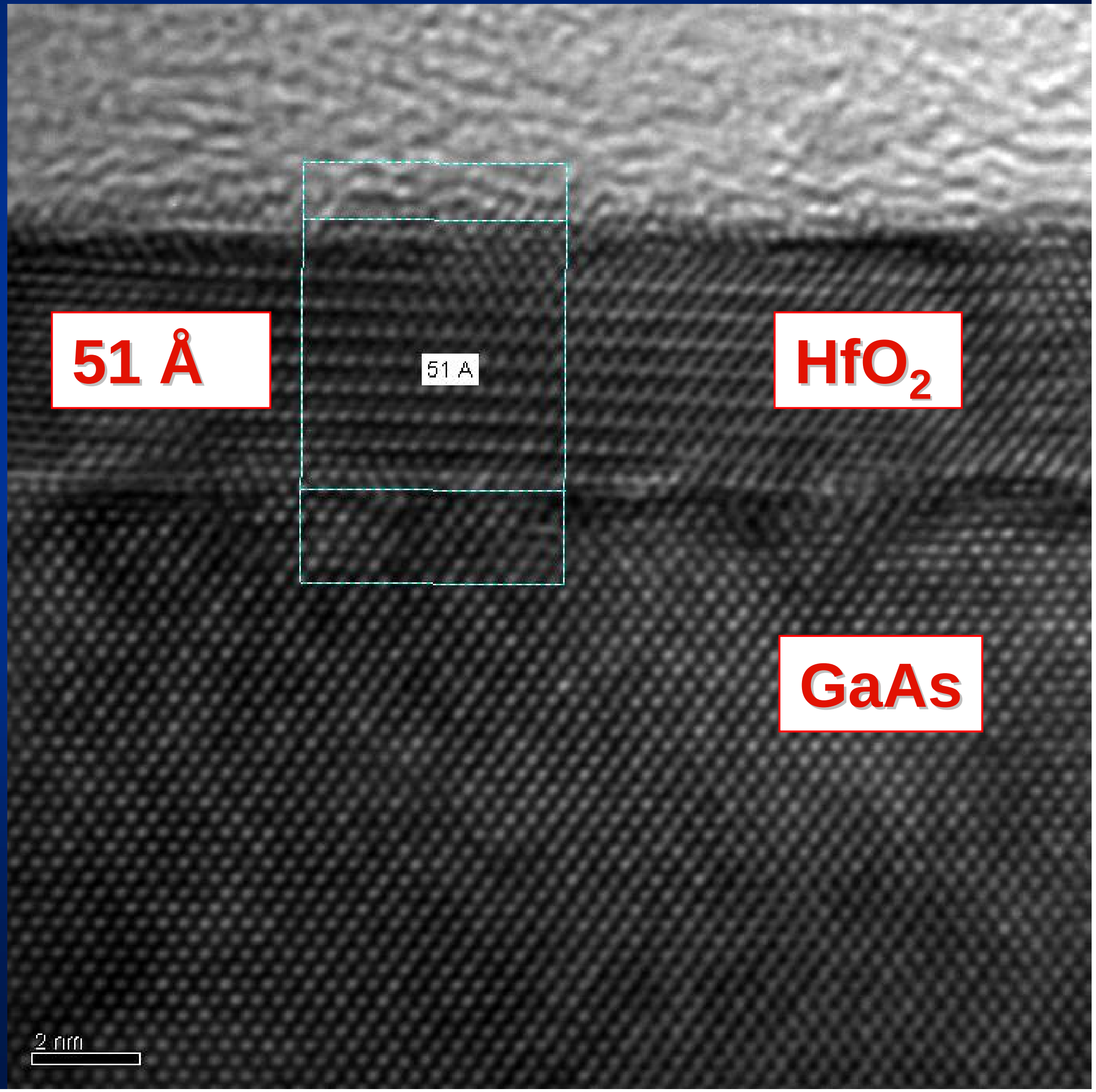
Epitaxial HfO_2 Films on GaAs

Amorphous + recrystalization + regrowth

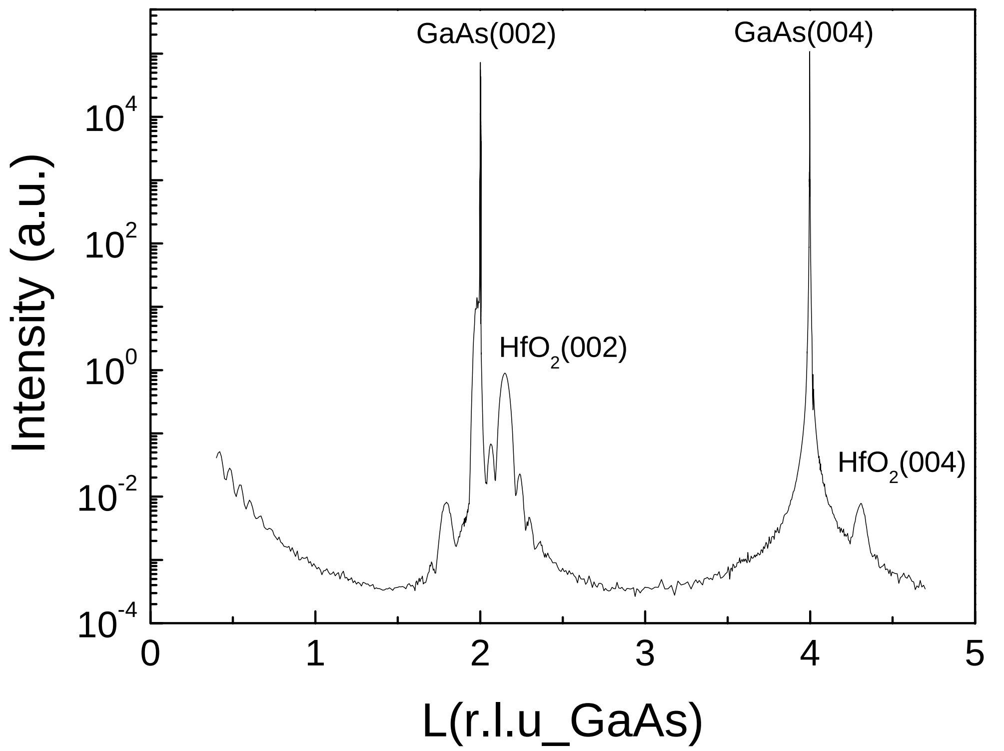
Cross Sectional HRTEM

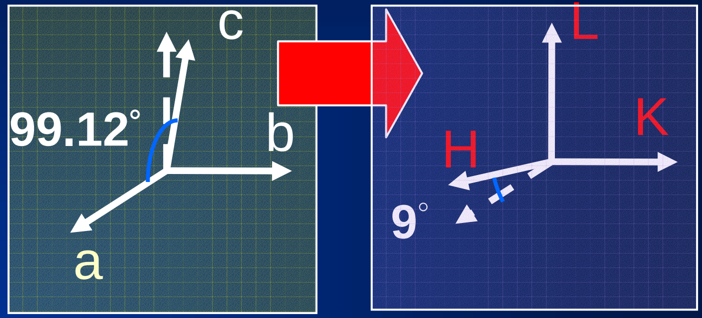
RHEED Pattern





X-ray Diffraction of Epitaxial HfO_2 Films Recrystalized on GaAs





R space

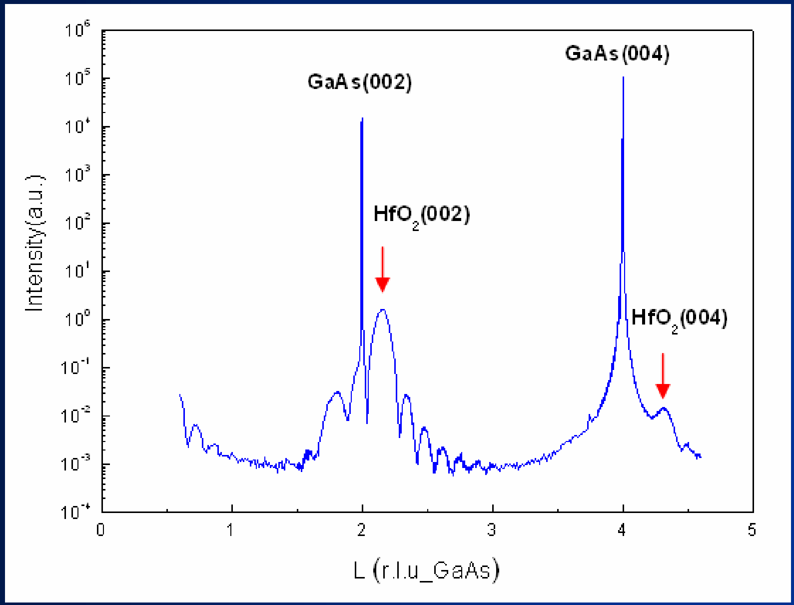
K space

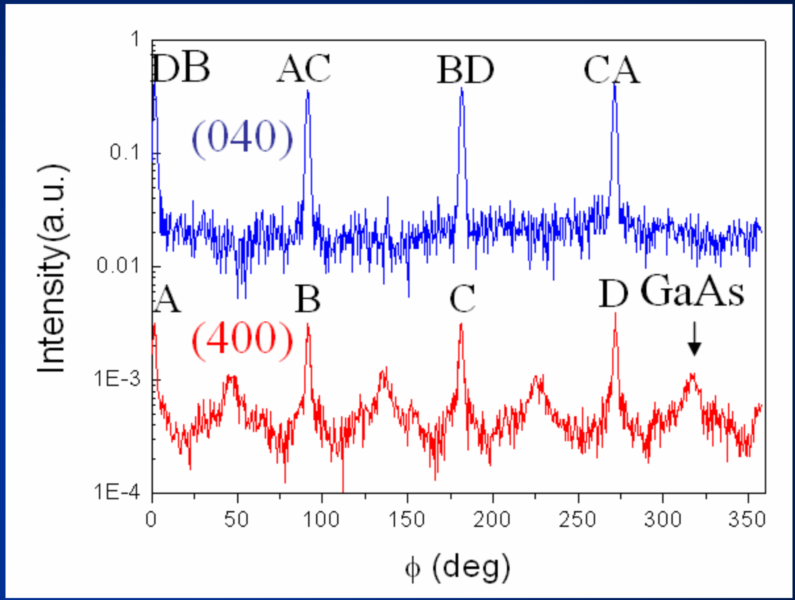
HfO_2(004) FWHM(L)=0.0578°
⇒ domain size 97.8 Å
⇒ close to film thickness

--- Monoclinic HfO_2 in R space and K space
--- Forming four degenerate domains about the surface normal

With C. H. Hsu of NSRRC

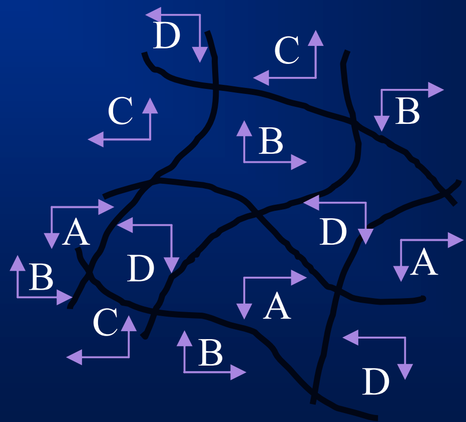
The Structure of HfO_2 Grown on GaAs(001)





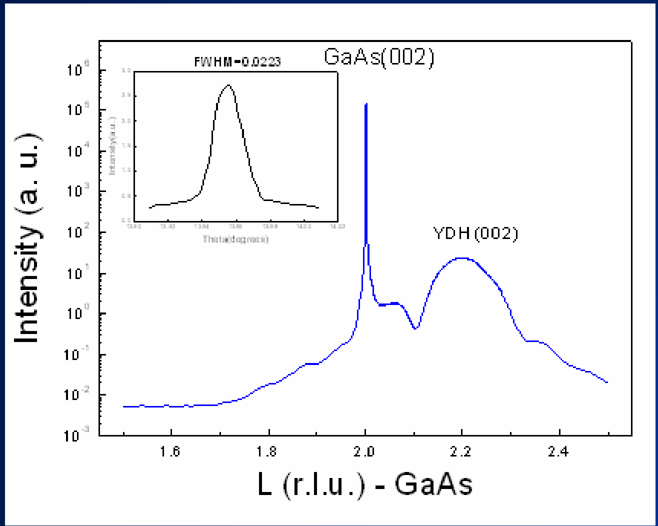
monoclinic phase

a=5.116A, b=5.172A, c=5.295A, β=99.18A



coexistence of 4 domains rotated 90º from each other

The Structure of HfO_2 doped with Y_2O_3 Grown on GaAs (100)



Surface normal scan

Find the peaks:

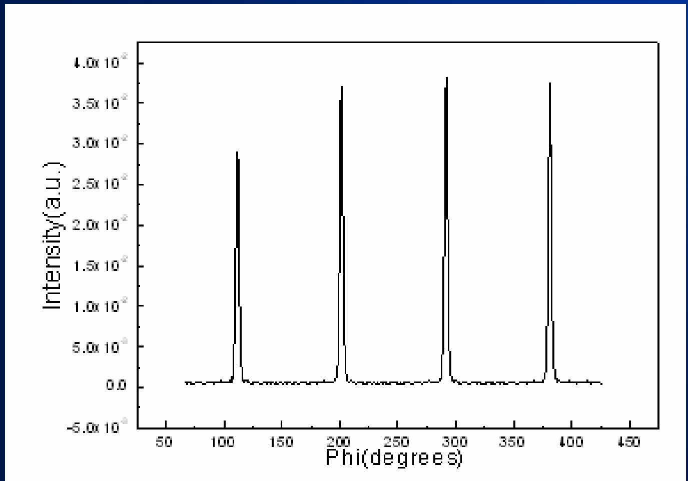
- (022)(400)(200)(311)(31-1)(113)(420)(133)(20-2)
- All peaks of film match the JCPDS of cubic phase HfO_2
- Use the d-spacing formula to fit the lattice parameters

→ HfO_2 doped with Y_2O_3 Grown on GaAs(001) is

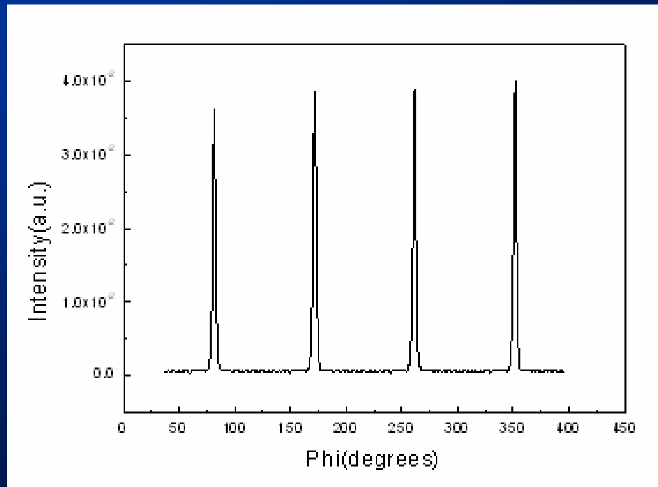
Cubic phase

a=5.126A, b=5.126A, c=5.126A

α=90, β=90, γ=90

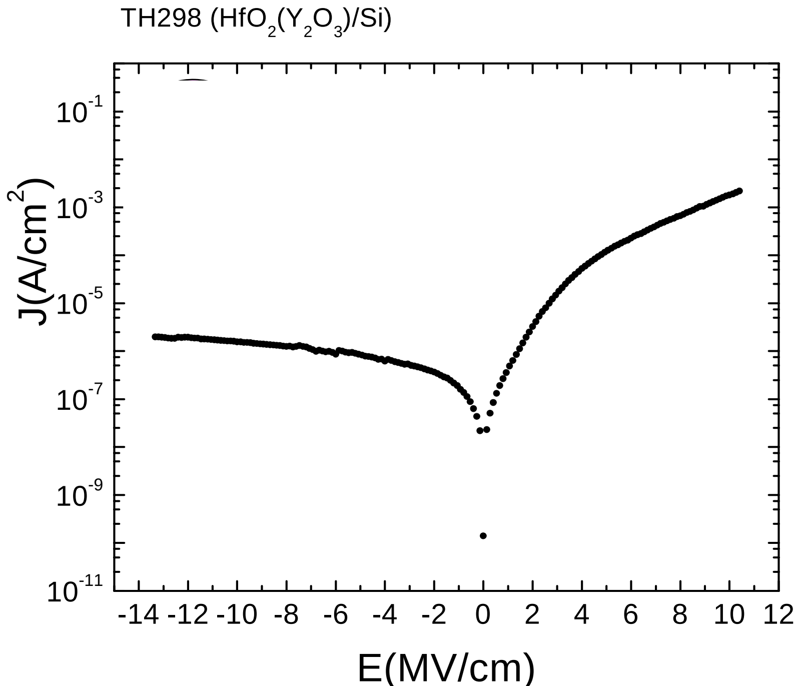


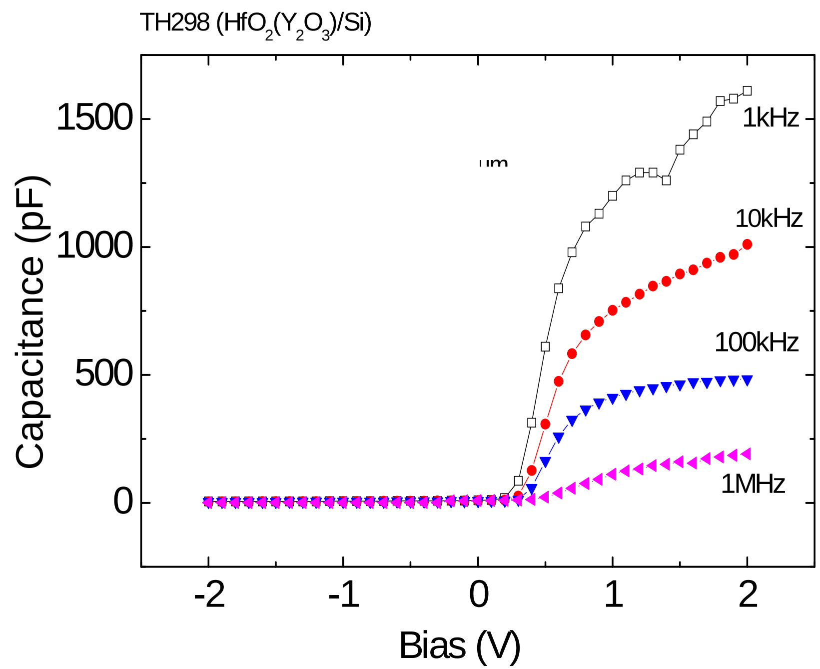
(400)Phi scan



(040)Phi scan

HfO_2 Doped with Y_2O_3 (~5 % level) Grown on Si





Using x-ray diffraction analysis at NSRRC,

*** A structure of the ***cubic*** phase through epitaxy, with a κ about **35** !!!

*** Removes the problem of thermal instability of HfO_2 at T > 550C

The Fermi Level Unpinning Mechanism of High κ oxide/GaAs interface

- Often found large flat band voltage shifts in C-V,
  --- fixed charges in oxides
- Presence of residual As-oxide near the oxide/GaAs interface
- Mechanism to remove the As-oxide from the oxide/GaAs interface
- Our recent work of passivation of III-V's surface using ALD - grown Al_2O_3

Electrical characterization / optimization

-- Good News !!

- **Low electrical leakage is common .**
- **Have Attained an EOT under 1.0-1.4 nm .**

-- Major problems are :

- High interfacial state density
- Large trapped charge
- Low channel mobility
- Electrical stability and reliability

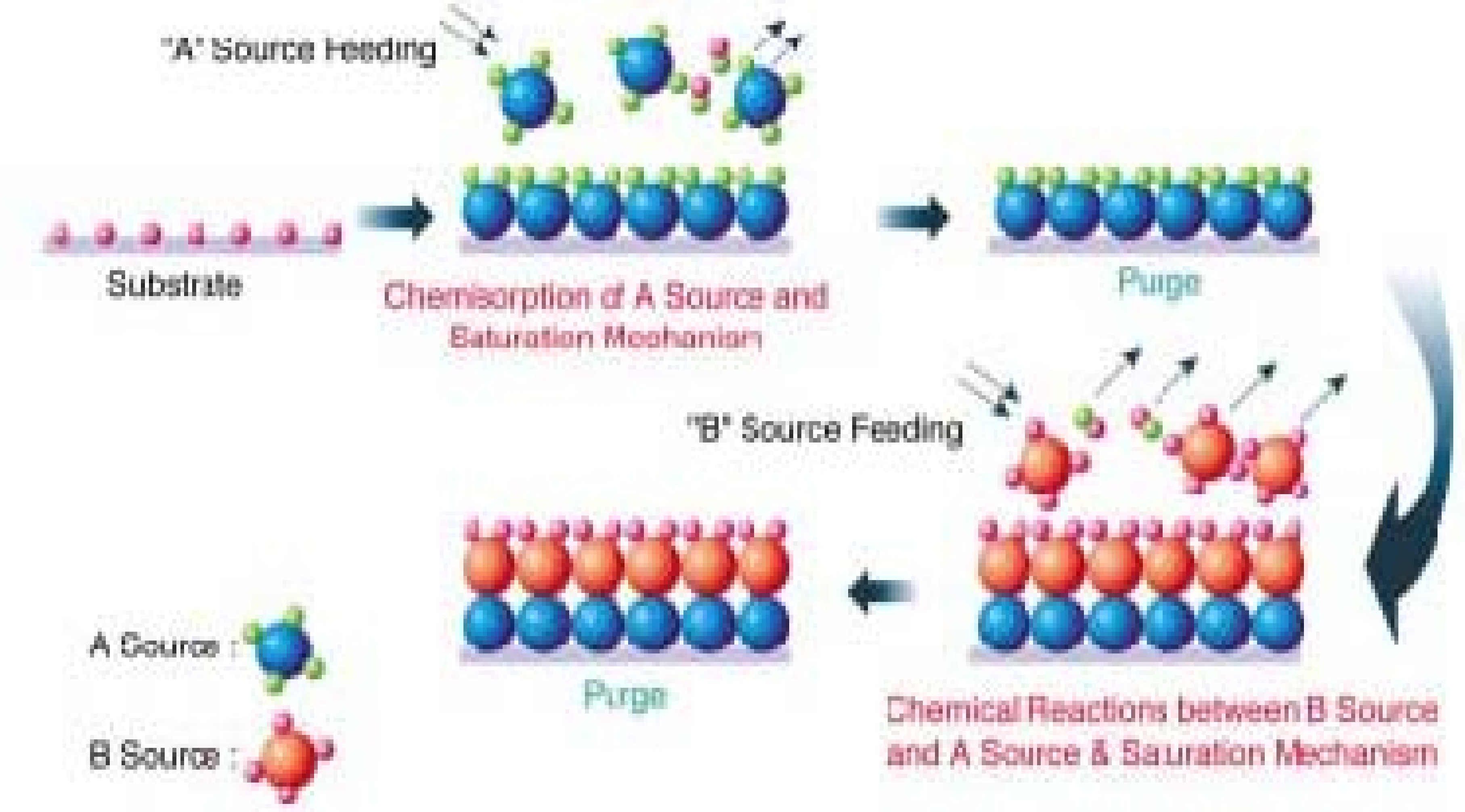
Difficulties of High κ MOSFET Fabrications

- Thermal stability of thin films
  - HfO_2 → Lowering the dopant activation temperature to 700°C
  - TiN → Using Ti/TiN bilayer structure
- Process integration
  - 4 inch Si (LOCOS)→2 inch Si (MBE)

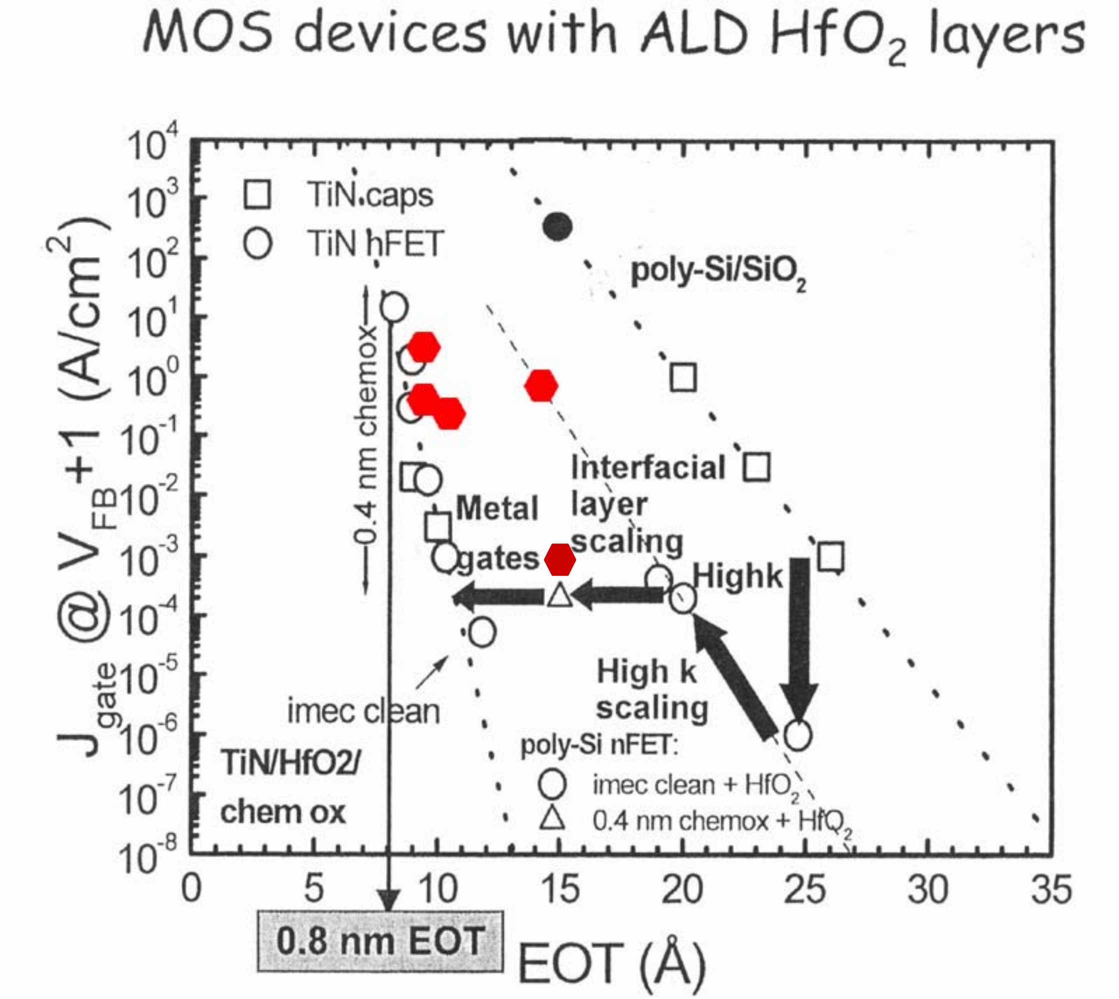
    → Successful integration

Atomic Layer Deposition (ALD)

Growth Mechanism : Formation of interfacial SiO_2 is hard to avoid.



Comparison between the MBE and ALD films



M. Houssa in Symposium D,
MRS Spring Meeting, April 12-16, 2004.

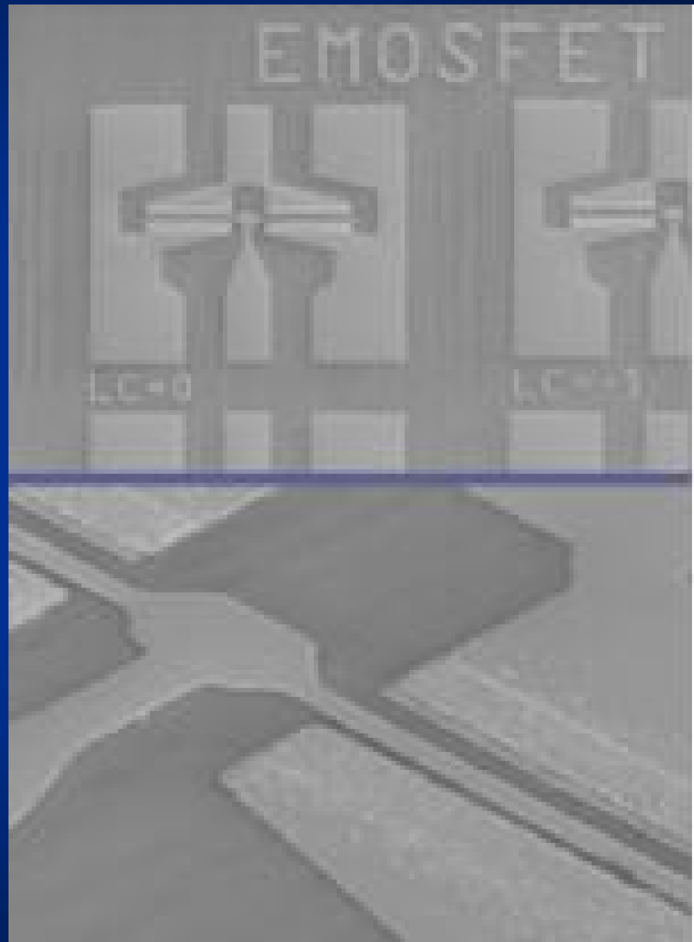
- MBE-grown Au/HfO_2/Si MOS diodes are denoted in red hexagons
- HfO_2 film 4.4 nm thick, with $J_L \sim 10^{-3}$ A/cm^2, κ of 20.7, an EOT of 0.9 nm
- t_{eq} = EOT

Equivalent Oxide Thickness

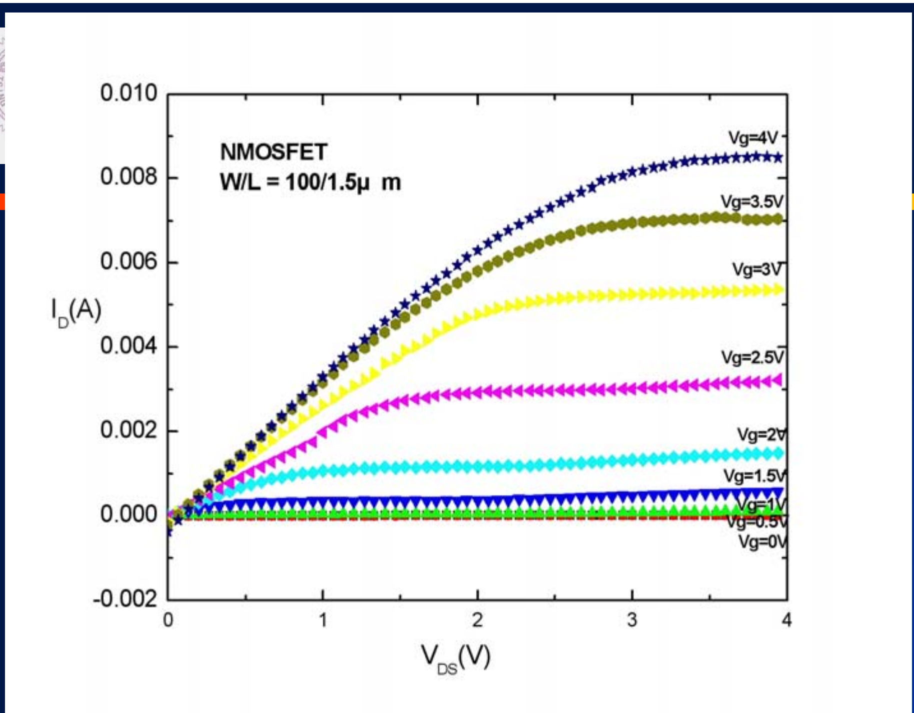
$$t_{eq} = t_{ox}\ \varepsilon_{SiO2} / \varepsilon_{ox}$$

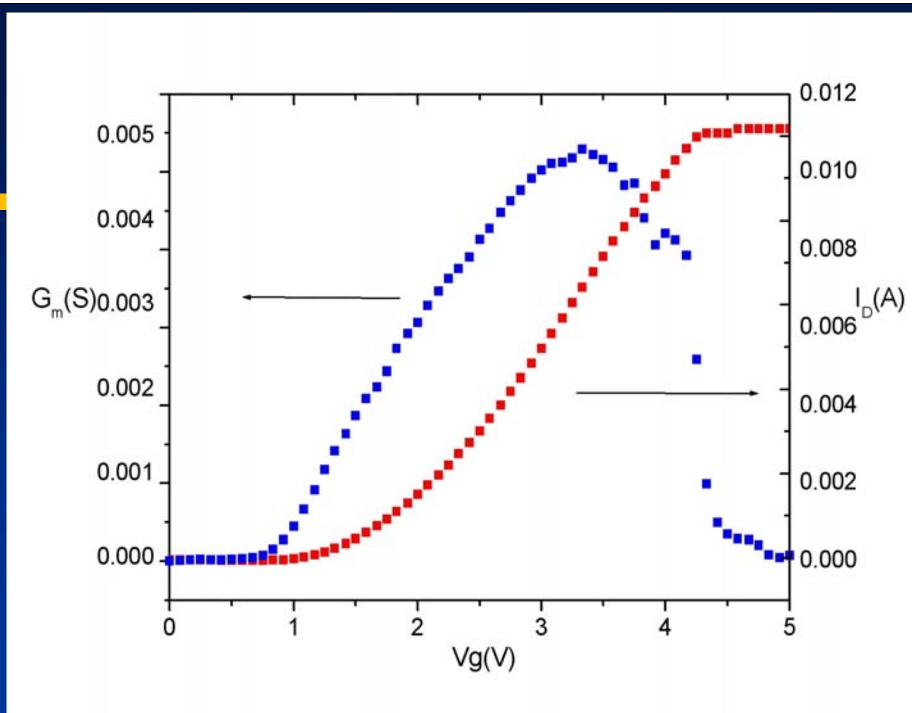
TiN/HfO_2/Si High κ MOSFET

- A self-sligned process
- With LOCOS isolation
- HfO_2 gate dielectrics
- TiN metal gate
- 2 inch MBE-grown high κ films
- A 4 inch Si line in ERSO for isolation
- A 6 inch Si line in NDL for processing



- W / L ~ 100 μm/ 1.5 μm
- EOT ~ 26 A (t_{ox} = 10 nm)
- I_d ~ 8.5 mA @ V_{gs} = 4V
- Gm = 48.5 mS/mm





- Activation temperature: 700°C
- Transconductance G_m is increased to 48.5 mS/mm, I_d ~ 8.5 mA W / L ~ 100 μm/ 1.5 μm, EOT ~ 2.6 nm.

Activation temperature (°C)	700	750	800	850
I_D@3.5V (mA)	7	1.9	1.2	1.2
G_m (mS/mm)	48.5	16	12	9
L_g (μm)	1.5	2	2	2

Comparison of the High κ Transistor Results

	NTHU	Intel 2003			Intel 2004
Structure	TiN/HfO_2 on Si	TiN/HfO_2			TiN/HfO_2
		Si	Strain-Si	Strain-Si	Si
L [um]	1.5	0.14	0.14	0.08	0.08
EOT [A]	26	?	?	?	14.5
Id [mA/mm]	85	500	625	930	1650
Gm [mS/mm]	48.5	660	750	1000	1750

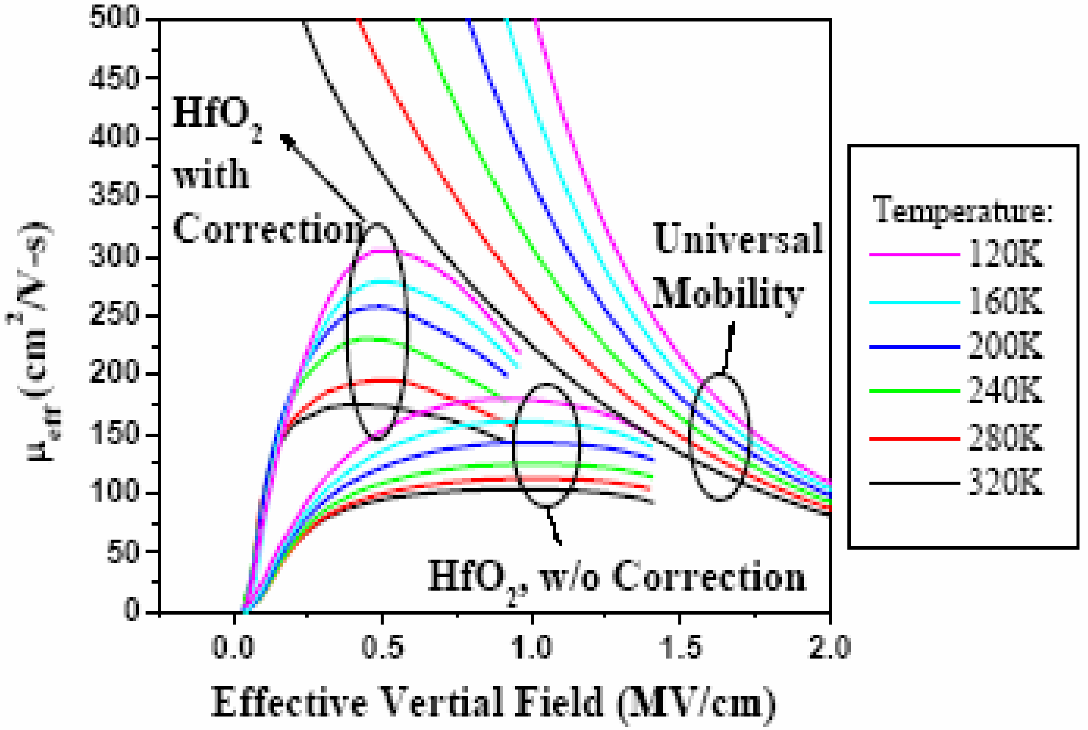
I_d/G_m = 50/66
when L = 1.5 um

I_d/G_m = 87.5/93
when L = 1.5 um

Considering the differences in L and EOT, our I_d and G_m are comparable to other leading groups.

Degradation of Mobility in High κ Gate Stack

Temperature dependence of mobility



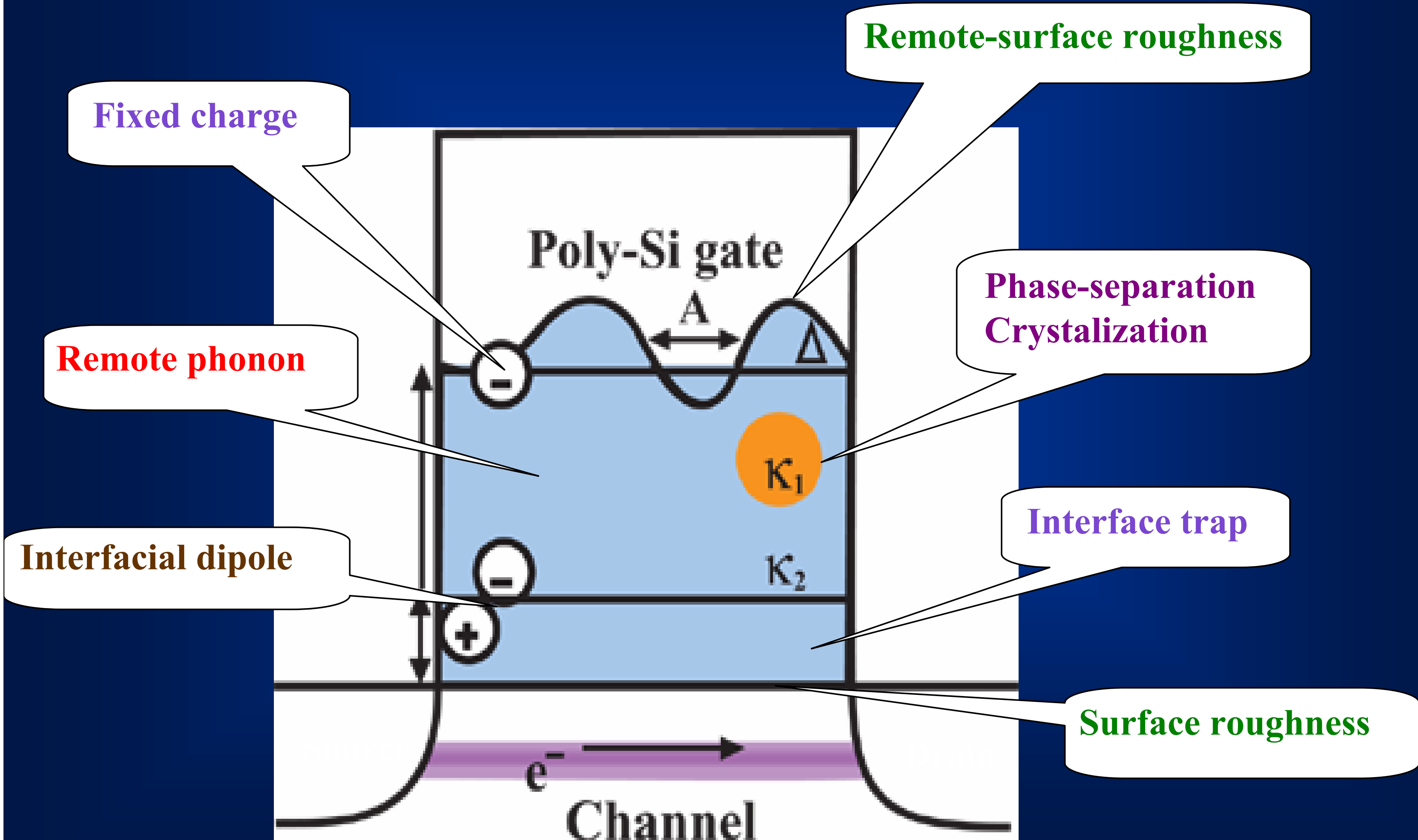
Correction from the charge trapping effect

- Effective mobility for HfO_2 is lower than universal mobility even after interface correction.

Phonons may have reduced mobility seriously !

Fechetti et al, JAP **90**, 4587, (2001).

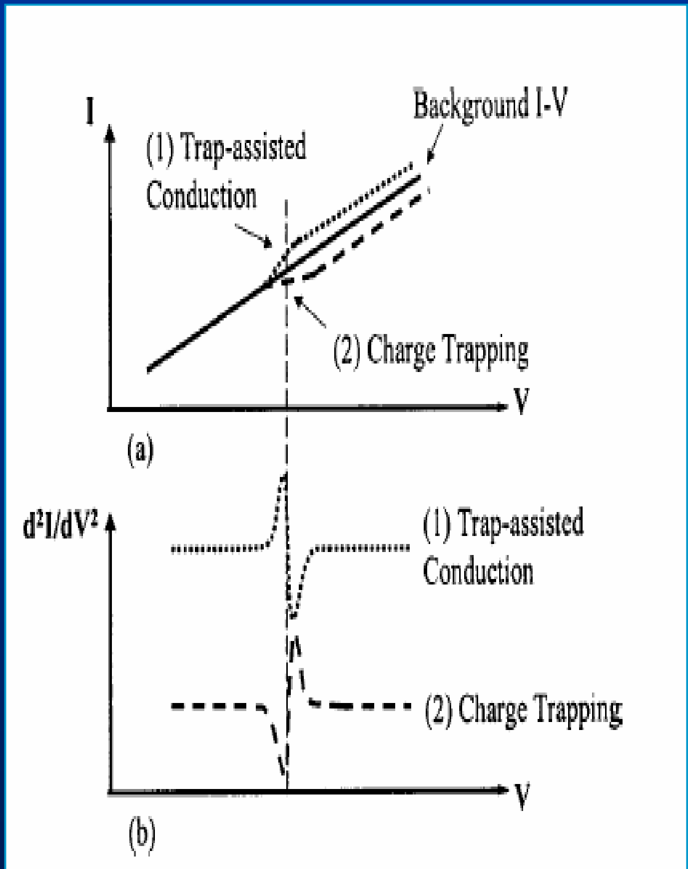
Possible Source of Mobility Degradation

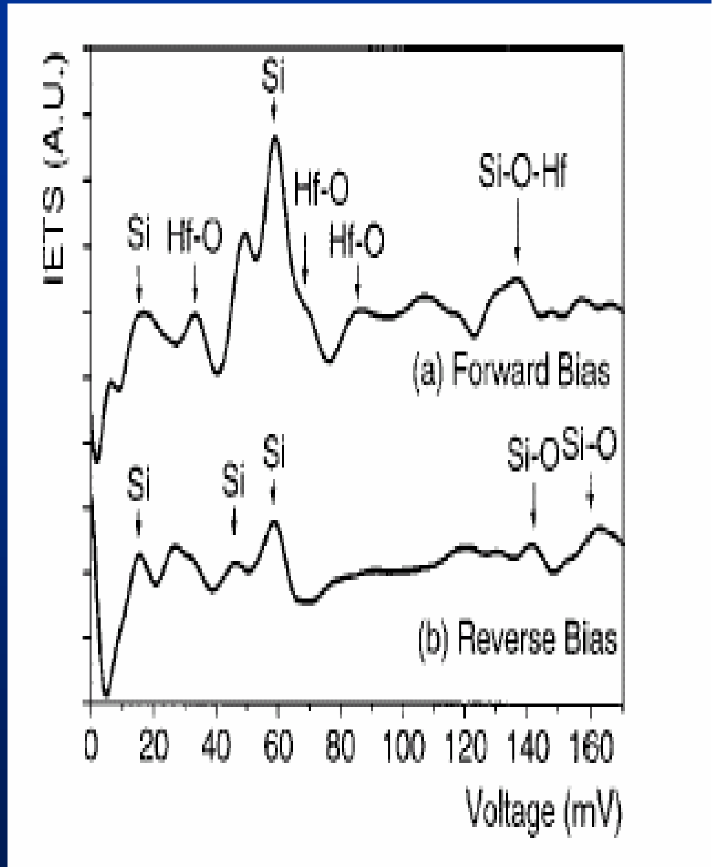


Inelastic Electron Tunneling Spectroscopy (IETS)

Charge trapping will cause shift in the threshold voltage.

Trap-assisted conduction will cause increased leakage current.



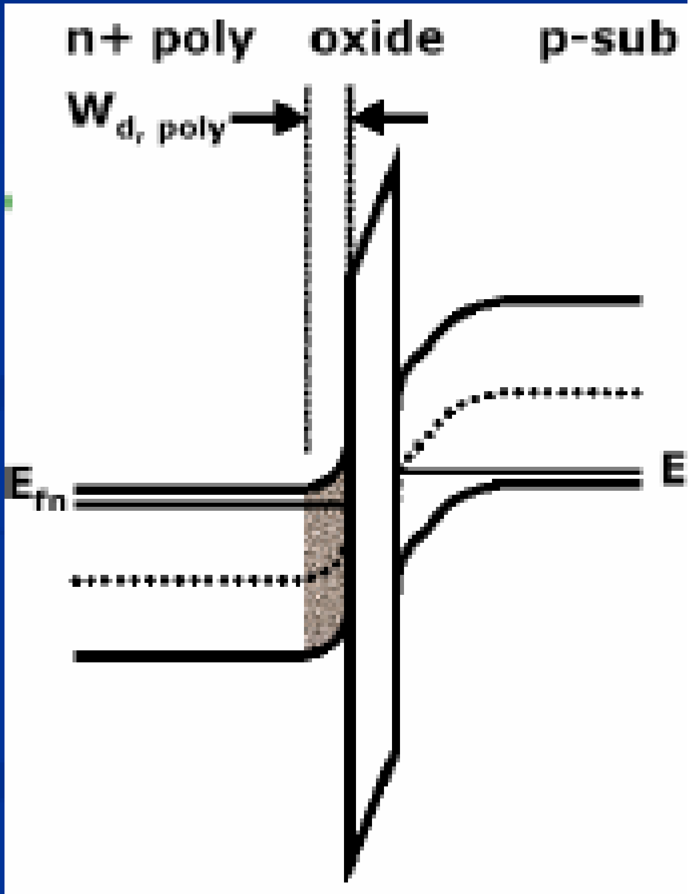


Wei He and T.P.Ma, APL **83**,2605, (2003) ; APL **83**, 5461, (2003)

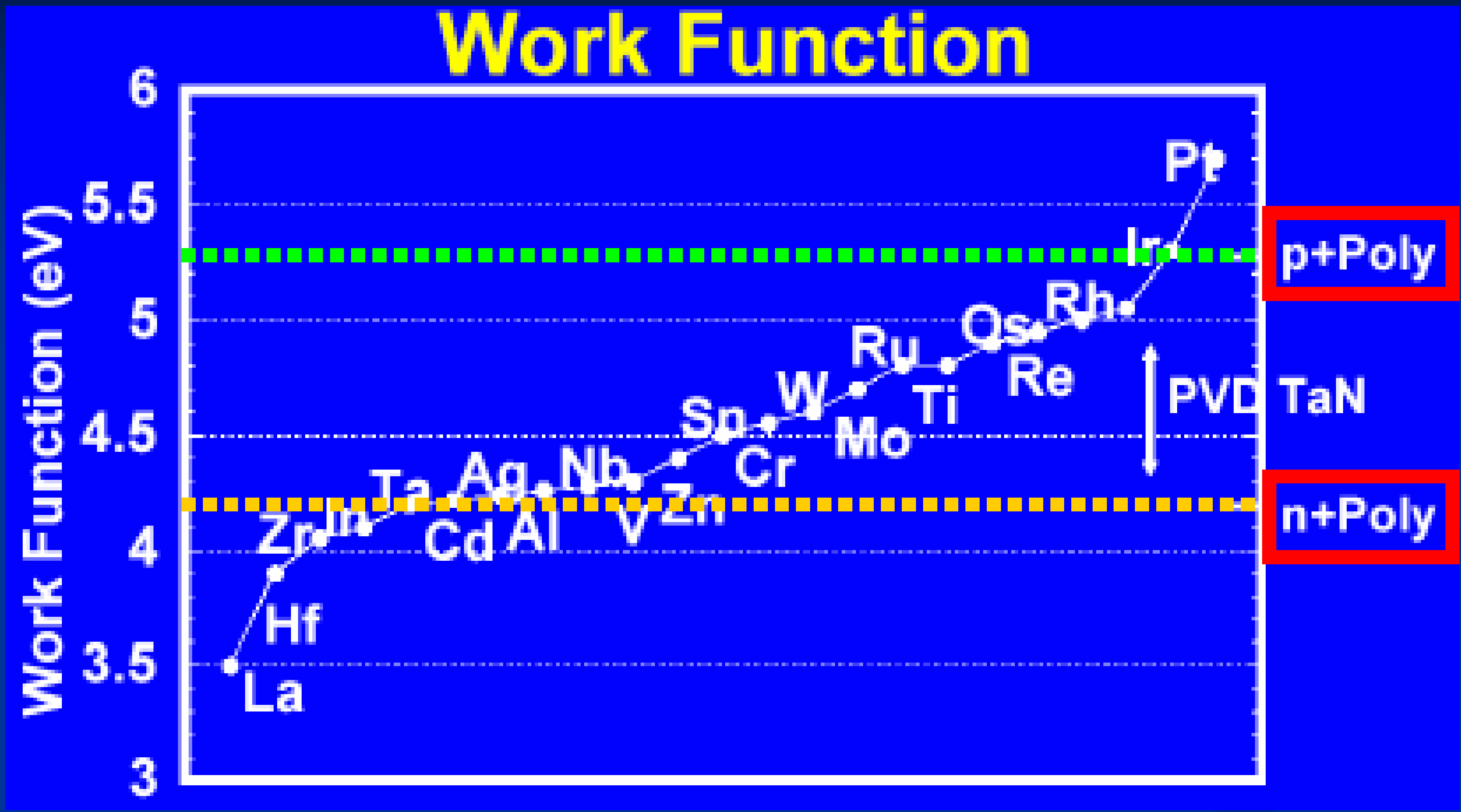
Metal Gate Electrode

- Probably implemented at 65 nm technology generation (2007) or beyond
- Advantages
  - No poly-depletion effects
    - 0.3-0.4 nm EOT reduction
  - No Boron penetration
  - Very low resistance
  - Large range of work function
  - Compatible with high-K gate dielectrics
  - Suppressed remote charge scattering
- Issues
  - Work function tuning to enable precise V_{th} control and minimize short-channel effects
  - Thermal stability at S/D activation
  - New materials: Major challenge

Poly-Si Gate Electrode



Metal Gate Electrodes for Dual-Gate CMOS



- Thermal stability of n-FET metal gate materials
- Metal nitrides
- Alloys
- Film structures

Major Research Accomplishment

- First demonstration of atomically abrupt high κ HfO_2/Si interface.
- First successful integration of the 6 inch Si CMOSFET processing in NDL with our 2” MBE high κ dielectric films using a TiN metal gate to produce a gate length 1.5 μm transistor device.
- Stablization of the ***cubic*** HfO_2 phase at 600°C to achieve an enahnced κ over 35.
- Effective passivation of the GaAs surface using high κ dielectrics HfO_2 in both amorphous and epitaxial forms with sharp interfaces.

HfO_2 High κ Dielectrics for GaAs Compound Semiconductor Passivation And MOSFET

New High κ Dielectrics for GaAs Passivation

- Advantages of compound semiconductor
  - High electron mobility
  - Semi-insulating substrate
  - High breakdown field
- A key challenge of device processing
  - Surface passivation
  - A novel oxide of low density of state (D_{it}) and low leakage
  - In-situ MBE growth of $Ga_2O_3(Gd_2O_3)$ ($\kappa = 12$) , and Gd_2O_3 ($\kappa = 14$)
- Sc_2O_3 /GaN successful passivation
- HfO_2 and Sc_2O_3 dielectrics for GaAs passivation

Novel High κ Dielectrics for III-V Semiconductors

III-V Semiconductor Surface Passivation
Searching for an insulators with low D_{it} and low leakage
MOSFET's for high speed, high power, and optoelectronic applications

--Discovery of a stable mixed oxide ***$Ga_2O_3(Gd_2O_3)$*** deposited on **GaAs** with low D_{it}
-- Epitaxy of single crystal (110) ***Gd_2O_3*** film on GaAs
-- Inversion-channel, E- and D-mode MOSFETs,

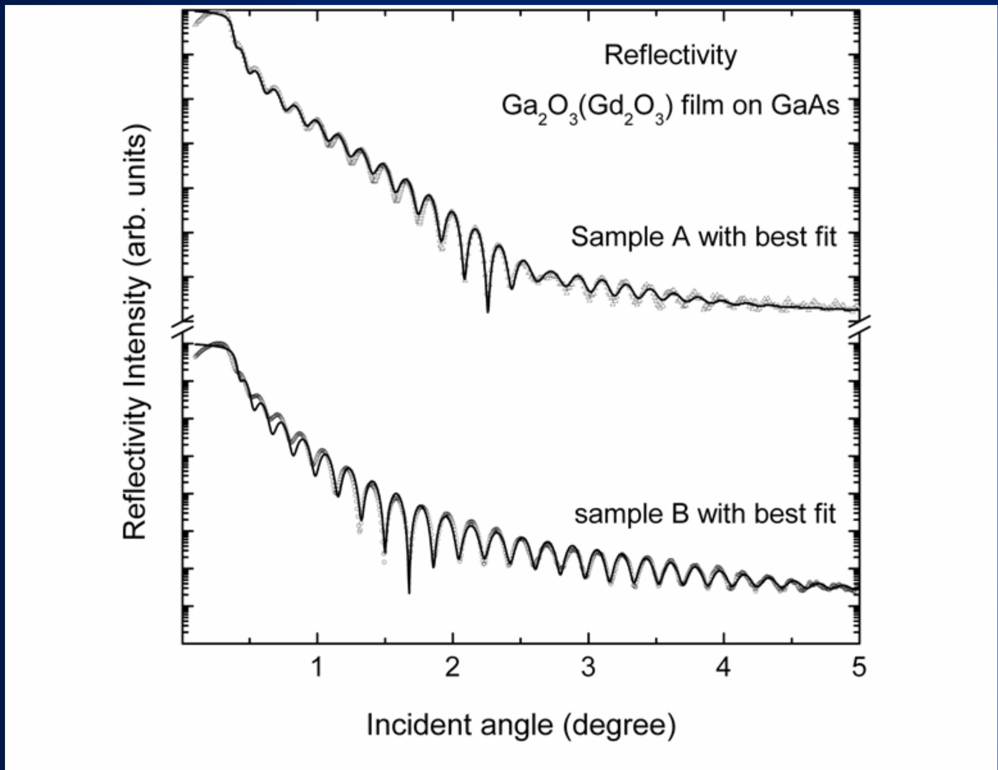
Have applied to other semiconductors such as InGaAs, AlGaAs, InP

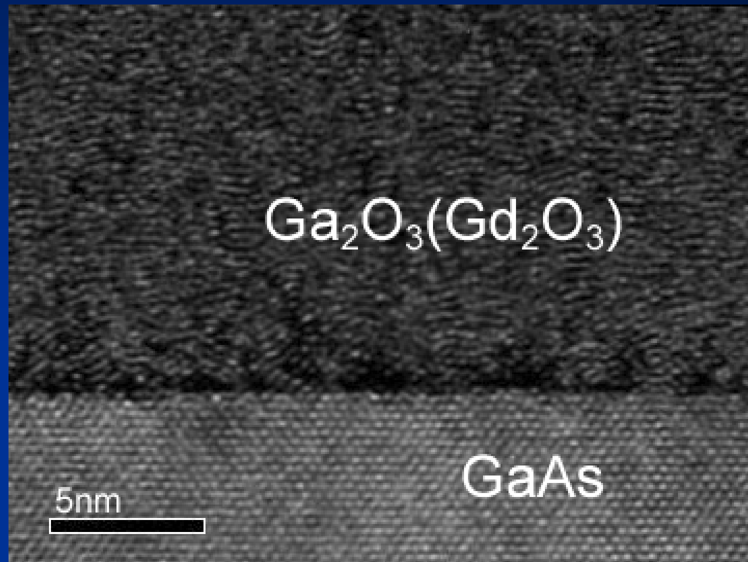
Growth of ***$Ga_2O_3(Gd_2O_3)$*** and (001)***Gd_2O_3*** on GaN
GaN/***Gd_2O_3***/GaN heteroepitaxy

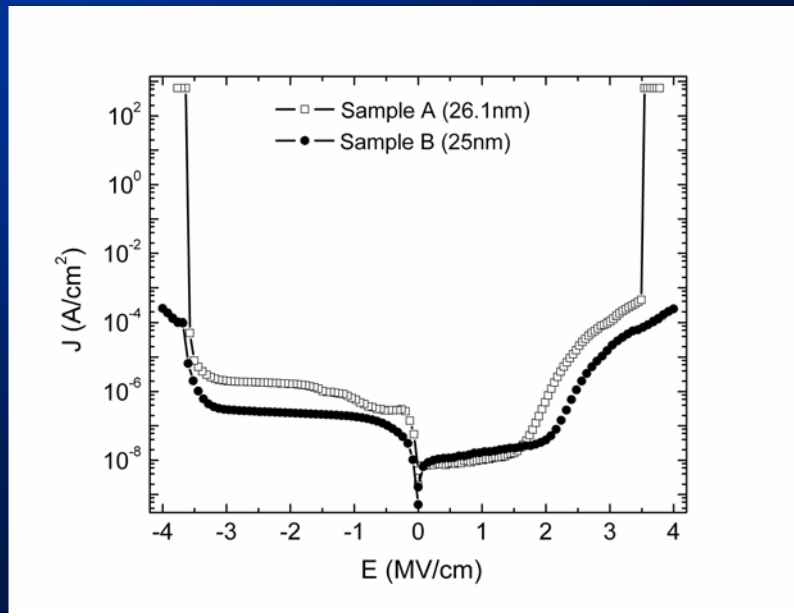
Inventions toward GaAs MOSFET's at Bell Labs

- 1994
  - novel oxide $Ga_2O_3(Gd_2O_3)$ to effectively passivate GaAs surfaces
  - demonstration of low interfacial recombination velocities using PL
- 1995
  - establishment of accumulation and inversion in p- and n-channels in $Ga_2O_3(Gd_2O_3)$-GaAs MOS diodes with a low D_{it} of 2-3 x 10^{10} cm^{-2} eV^{-1}(IEDM)
- 1996
  - first e-mode GaAs MOSFETs in p- and n-channels with inversion (IEDM)
  - Thermodynamically stable
- 1997
  - e-mode inversion-channel n-InGaAs MOSFET with g_m= 190 mS/mm, and mobility of 470 cm^2/Vs (DRC, EDL)
- 1998
  - d-mode GaAs MOSFETs with negligible drain current drift and hysteresis (IEDM)
  - e-mode GaAs MOSFETs with improved drain current (over 100 times)
  - Dense, uniform microstructures; smooth, atomically sharp interface; low leakage currents
- 1999
  - GaAs power MOSFET
  - Single-crystal, single-domain Gd_2O_3 epitaxially grown on GaAs
- 2000
  - demonstration of GaAs CMOS inverter
- 2001-2002
  - Design of high-speed and high-power devices; reliability of devices

$Ga_2O_3(Gd_2O_3)$/GaAs Heterostructures



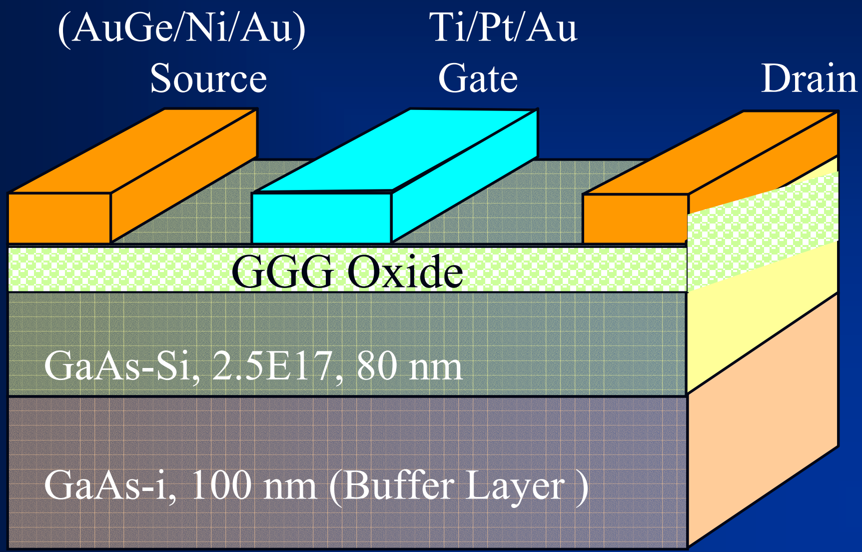


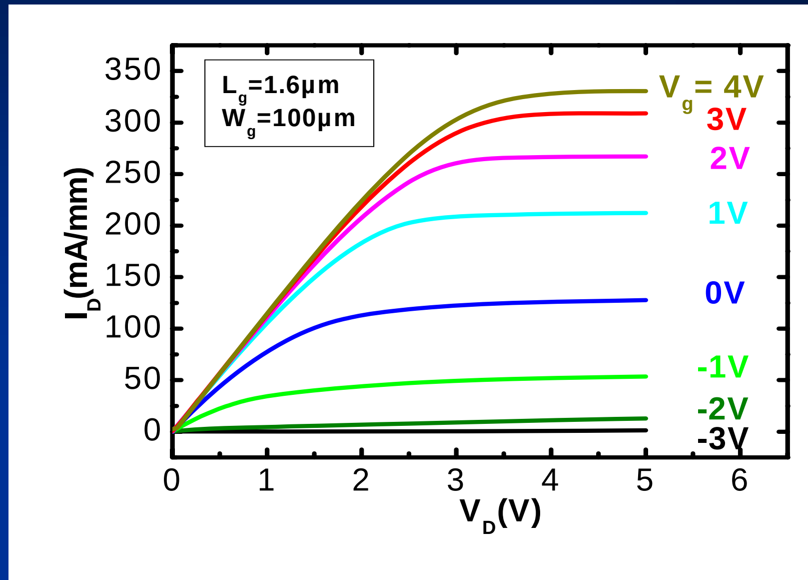


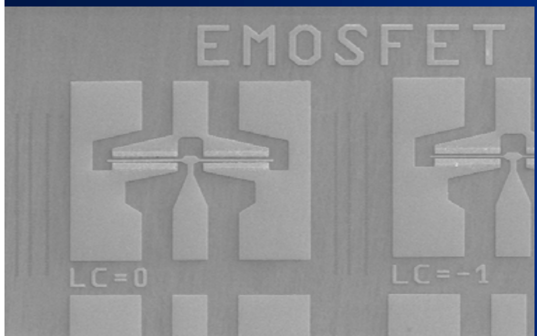
The oxide films remained amorphous with a sharp interface after 780°C anneal.

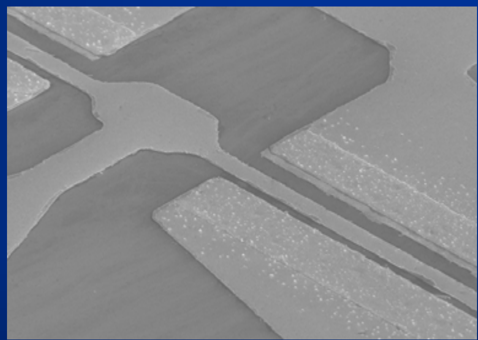
$\kappa = 15$

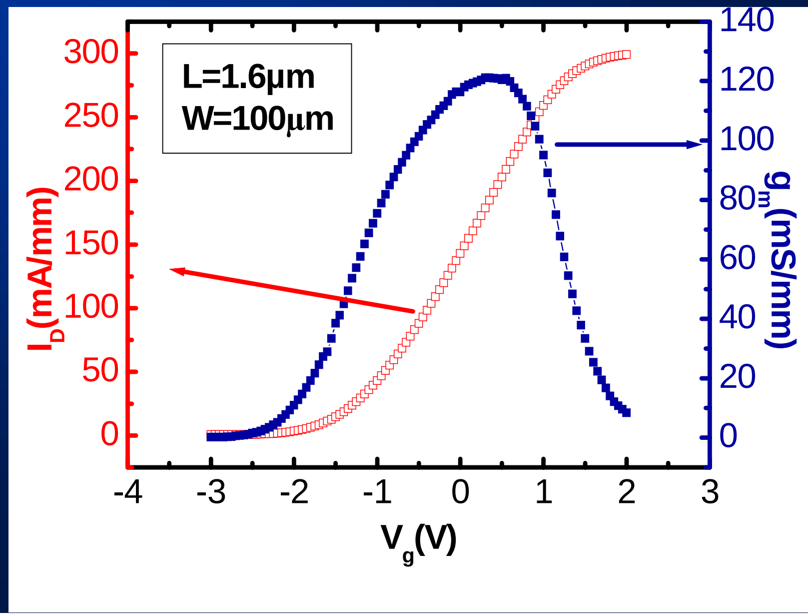
D-mode GaAs/InGaAs MOSFET with $Ga_2O_3(Gd_2O_3)$ as a Gate Dielectric











- 1.6 μm gate-length
- 335 mA/mm
- 120 mS/mm
- With $In_{0.15}Ga_{0.85}As$, 171 mS/mm